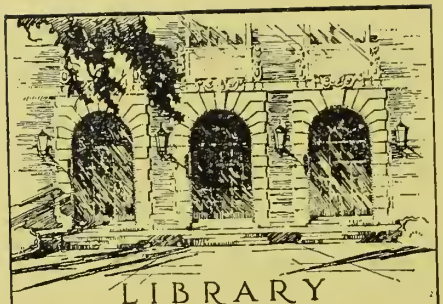

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DEPARTMENT OF COMPUTER SCIENCE · UNIVERSITY OF ILLINOIS · URBANA, ILLINOIS

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ARTRIX FINAL REPORT

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LIST OF ILLUSTRATIONS - APPENDIX

1.0 General Description

1.1 Purpose

ARTRIX is a graphical processing system which assimilates information in the form of points indicated on a DISPLAY with a LIGHT PEN, and produces graphical constructions on the DISPLAY at the command of the operator. Any geometric constructions which are possible on paper using a straight edge and compass may be accomplished and stored on the ARTRIX DISPLAY. Constructing a line through two points or a circle about a center point with a given radius are two typical constructions for which ARTRIX may be used. In addition, any freehand line drawings may be written on the DISPLAY with the LIGHT PEN and stored. Local erasure of constructions and drawings is also possible. Digital outputs are easily provided, thus enabling ARTRIX to be used as an on-line processing system in conjunction with a computer.

The general purpose of the ARTRIX system - conceived by Professor Poppelbaum - is to demonstrate the feasibility of a self-contained processing system, that is, a system which does not require a large digital computer for information processing and storage. In addition, ARTRIX is a feasibility study of a hybrid system, hybrid in the sense that it contains both analog and digital circuitry, and combinations thereof.

1.2 Physical Description and Definition of Subsystems

Figure 1.1 shows the entire ARTRIX system with each main component labelled. Figures 1.2 through 1.4 show the main components of ARTRIX, individually.

ARTRIX consists, basically, of the following subsystems: the PROCESSOR, the MEMORY, and the DISPLAY. Figure 1.5 is a block diagram of ARTRIX showing the interconnections between subsystems.

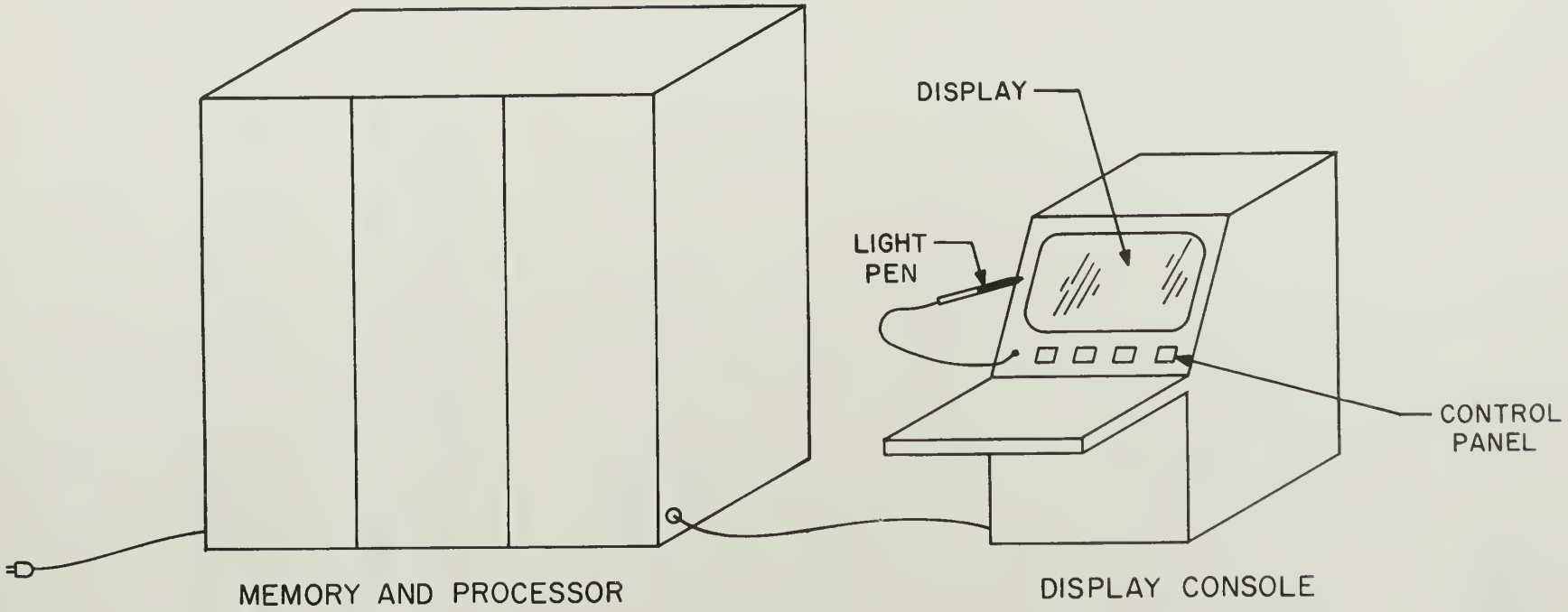


Figure 1.1 The ARTRIX System

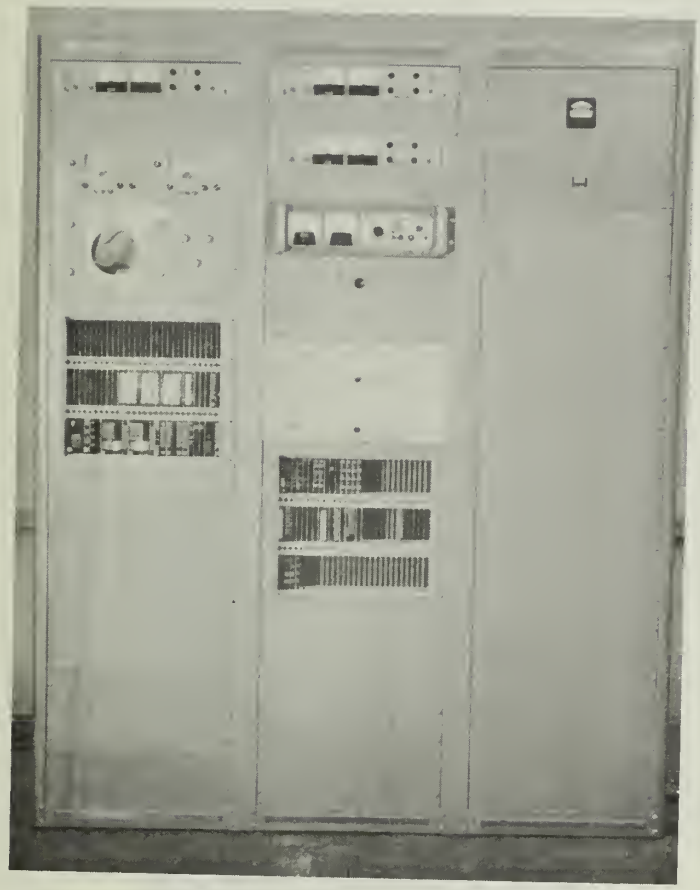


Figure 1.2 MAIN CONSOLE

Figure 1.3 a DISPLAY CONSOLE, Front

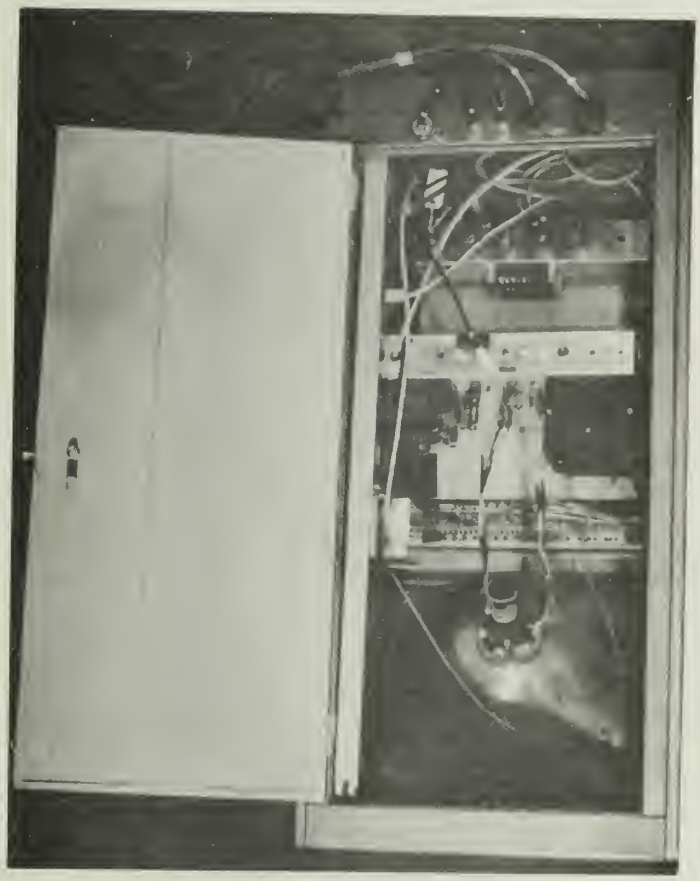


Figure 1.3 b DISPLAY CONSOLE, Rear

Figure 1.4 LIGHT PEN

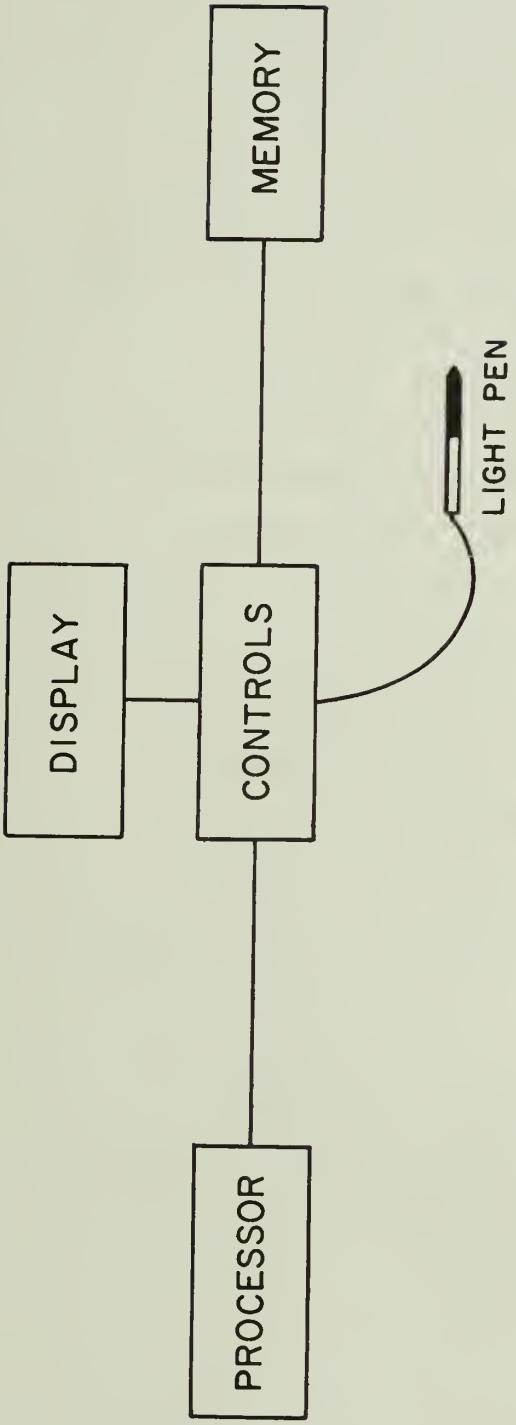


Figure 1.5 Block Diagram of ARTRIX

The PROCESSOR and MEMORY are contained in the MAIN CONSOLE (Figure 1.2). The PROCESSOR is a hybrid subsystem, containing all the digital logic and hybrid circuitry necessary for the graphical constructions. The MEMORY contains four analog storage units necessary for storing construction points, for storing line drawings on the DISPLAY and for use during the ERASE mode of operation. These four units are called the TEMPORARY, ERASE, POINT and DISPLAY memories.

The DISPLAY, which is contained in the DISPLAY CONSOLE, is a television monitor which serves as the "writing pad" for the operator (Figure 1.3). On it, he draws all his line drawings, performs graphical constructions, and erases when he so desires.

In addition to the three basic subsystems, the LIGHT PEN and CONTROLS are integral parts of the system, though they are not classified as subsystems. The LIGHT PEN (Figure 1.4) plugs into the DISPLAY CONSOLE, and in the WRITE mode of operation it is used as an ordinary pencil except that an actuating button called the ENABLE button must be depressed. In the ERASE mode of operation the LIGHT PEN is used as an eraser in a similar manner.

The CONTROLS consist of rows of buttons on the DISPLAY CONSOLE which switch the system between the various modes of operation. Above each button is an indicator which lights when the system switches to the chosen mode of operation or when the indicated function has been performed.

1.3 Description of Operation

The three basic modes of operation of ARTRIX are WRITE, CONSTRUCT and ERASE. The following paragraphs describe the sequences of operation in each of these three modes. It is assumed that the system has been switched on and that sufficient warm-up time has been allowed.

1.3.1 The WRITE Modes

The operator may write in either the WRITE DISPLAY mode or the WRITE POINT mode. The former is for simple line drawings while

the latter is for writing construction points. Both the points written in the WRITE POINT mode and the line drawings written in the WRITE DISPLAY mode appear simultaneously on the DISPLAY as well as any constructions which have been performed. Depressing the appropriate button will switch ARTRIX to the chosen mode of operation. Refer to Figure 1.6. The writing of either points or line drawings is then accomplished by depressing the ENABLE button on the LIGHT PEN and writing with the LIGHT PEN on the DISPLAY as one would write with a pen on paper.

1.3.2 The CONSTRUCT Mode

Assuming that several points have been written in the WRITE POINT mode, the operator may wish to proceed with a construction. Depressing the button labelled CONSTRUCT places the system in the CONSTRUCT mode of operation. The operator must then select the desired mode of construction, circle or line, and depress the appropriate button. Two points are required for the construction of a line or circle. For a line the two points are its end points and for a circle the two points are, in sequence, the center of the circle and a point on its circumference. Of the points which have been written in the WRITE POINT mode, the two which are to be used for the construction must be indicated with the LIGHT PEN. When the LIGHT PEN is directed to the first point, and the ENABLE button depressed, the POINT 1 STORED indicator will light. Similarly, when the second point is selected with the LIGHT PEN, the POINT 2 STORED indicator will light. If ARTRIX is in the CIRCLE mode of operation, the RADIUS STORED indicator will light soon after the two points have been selected. The construction is executed upon depressing the EXECUTE CONSTRUCT button. A straight line will then appear between the two points in the LINE mode of operation, or a CIRCLE will appear centered at the first point with the second point on its circumference in the CIRCLE mode of operation.

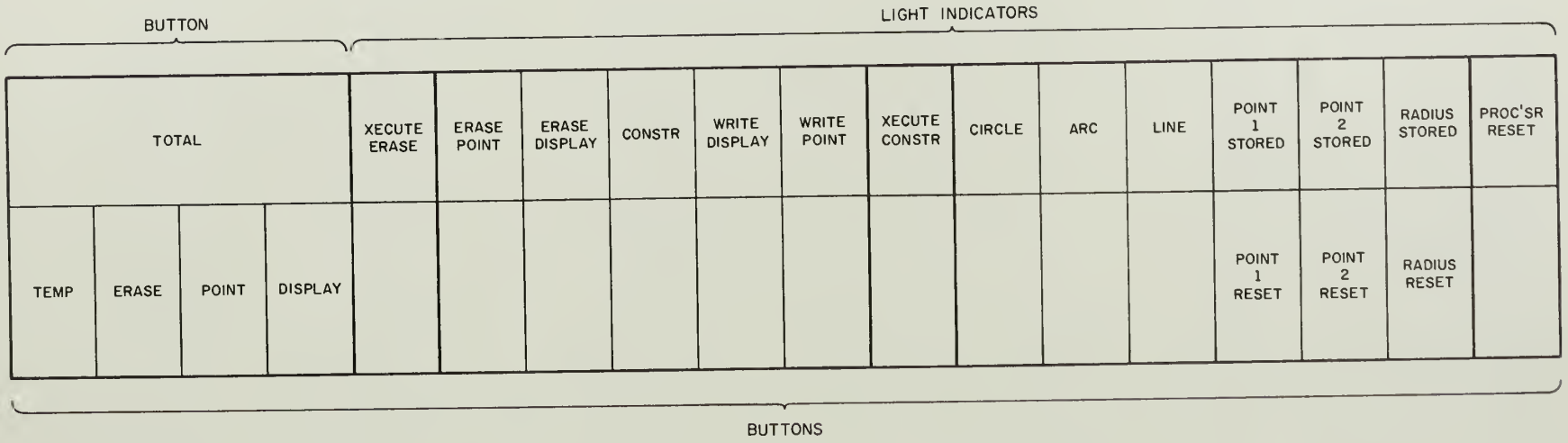


Figure 1.6 Controls of ARTRIX

In addition to the basic operations described above, ARTRIX is capable of translating circles and lines as well as constructing concentric circles. These operations are accomplished, basically, by indicating a new point to replace one of the two used previously in a construction.

Translation of circles is accomplished by depressing the POINT 1 RESET button and indicating a new POINT 1 with the LIGHT PEN. The POINT 1 STORED indicator will light again indicating that a circle is to be constructed about the new center point with the same radius as that of the previous circle. Upon depressing the EXECUTE CONSTRUCT button, a new circle will appear in addition to the one previously constructed, but which has been translated to the new center.

A line which has been constructed in the LINE mode of operation may be translated parallel to itself by depressing the POINT 1 RESET button and indicating a new POINT 1 with the LIGHT PEN. When the EXECUTE CONSTRUCT button is depressed, a line will appear on the DISPLAY parallel to the first line, terminating at the new POINT 1. Its length will be the same as that of the first line.

Concentric circles are constructed by changing POINT 2 and the radius of the first circle. The POINT 2 RESET button and the RADIUS RESET button must be depressed and a new POINT 2 indicated with the LIGHT PEN. The distance between this and POINT 1 will, of course, be the new radius. When POINT 2 is indicated, the POINT 2 STORED indicator and RADIUS STORED indicators will light. Upon depressing the EXECUTE CONSTRUCT button, a new circle will appear concentrically about or within the first circle.

If an entirely different construction is to be performed, depressing the PROCESSOR RESET button will clear the PROCESSOR of points used previously in constructions. The PROCESSOR RESET indicator will light when the PROCESSOR has been reset.

The PROCESSOR may be reset even though ARTRIX is not in the CONSTRUCT mode. However, no new points may be indicated and stored until the system is returned to the CONSTRUCT mode. In addition, the PROCESSOR preserves all stored information when ARTRIX is switched in and out of the CONSTRUCT mode.

1.3.3 The ERASE Modes

ARTRIX is equipped with facilities for erasing partially, for example, erasing sections of a line drawing; or erasing totally, that is, erasing the entire contents of one or all of the four storage units of the MEMORY. Buttons designating erasure of each of the four units, TEMPORARY, ERASE POINT, and DISPLAY, are located on the CONTROL switch panel. Depressing any one of these will erase the entire contents of the corresponding storage unit. Depressing the button labelled TOTAL will erase the contents of all of the four storage units, thus clearing the entire MEMORY of previously stored information.

Either the POINT memory or the DISPLAY memory may be erased selectively by depressing the button labelled ERASE POINT or ERASE DISPLAY, respectively. The portions of the line drawing or the points to be erased must be indicated with the LIGHT PEN. The LIGHT PEN is used as if it were an eraser, with the ENABLE button depressed. When all points or lines to be erased have been so indicated, these points and lines will vanish from the DISPLAY upon depressing the button labelled EXECUTE ERASE.

2.0 Subsystem Interaction

Figure 2.1 shows the basic interconnections between the PROCESSOR, MEMORY, and DISPLAY subsystems of ARTRIX. The PROCESSOR is shown in two separate blocks, one representing the digital section, the other representing the hybrid section. The TEMPORARY memory has been deleted from the MEMORY block since it operates in conjunction with the ERASE and DISPLAY memories only, and does not interact with the other subsystems. Also shown in Figure 2.1 is the LIGHT PEN as well as those switches relevant to the subsystem interaction. Included in this section of the report are brief discussions of the MEMORY and PROCESSOR to facilitate an understanding of the subsystem interaction. Detailed discussions of these subsystems follow in Sections 3.2 and 3.3.

Each of the four storage units of the MEMORY, namely DISPLAY, POINT, ERASE and TEMPORARY (the latter having been deleted) consists of a storage tube for storage of information, and a Vidicon camera for reading the stored information. A deflection signal is necessary for controlling the WRITE beam of the storage tube. Each memory is also equipped with an erase input for erasing its entire contents. Thus there are three inputs and one input from each unit; the inputs are the write, deflection and erase signals, and the output is the read signal. These signals are labelled W, D, E, R, respectively, on Figure 2.1. Only those inputs and outputs relative to the discussion are shown in Figure 2.1. In the WRITE DISPLAY mode of operation switch S_2 is set at position 1, and the signal from the LIGHT PEN is directed to the WRITE input of the DISPLAY memory. Thus the sketch is stored in the DISPLAY memory as it is being drawn. S_3 is normally switched to the position labelled NORMAL DEFLECTION, ganged with S_1 which is normally open.

Similarly, with S_2 in position 2, and the system in the WRITE POINT mode, points are drawn with the LIGHT PEN and stored in the POINT MEMORY. With S_2 in position 3, and ARTRIX in the ERASE mode, all points or portions of a drawing indicated for erasure with the LIGHT PEN are stored in the ERASE MEMORY. When points are to be erased from the

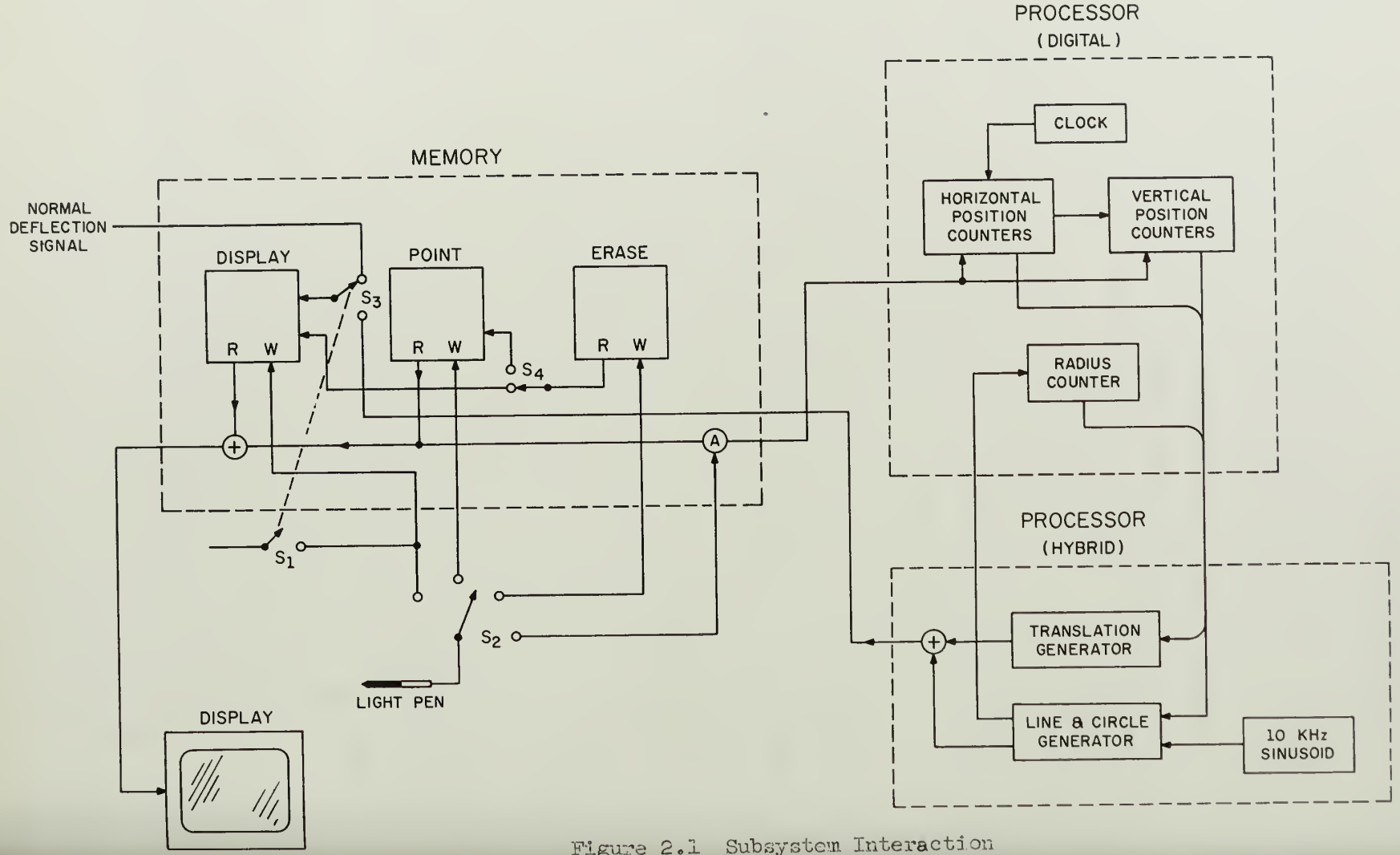


Figure 2.1 Subsystem Interaction

POINT MEMORY, S_4 will be in the upper position; when portions of a sketch are to be erased from the DISPLAY MEMORY, S_4 will be in the lower position.

The DISPLAY consists of a cathode ray tube whose beam sweeps out the stored information on the MONITOR. The LIGHT PEN contains a photosensitive device which detects the light of the beam as it sweeps in front of the pen. The time which elapses between the beginning of the sweep and the instant when the beam position and pen position are coincident is a measure of the coordinate position of the LIGHT PEN on the DISPLAY. Coincidence is detected by the AND gate when S_2 is in position 4, as shown in Figure 2.1. When signals appear at the input of the gate simultaneously, a signal will appear at the output.

The digital section of the PROCESSOR contains binary counters whose contents correspond to vertical and horizontal coordinates of the position on the DISPLAY. These counters run continuously in synchronization with the motion of the electron beam in the DISPLAY until a point is indicated. That is, each binary count in the vertical counter corresponds to one of 500 horizontal lines on the DISPLAY, and each binary count in the horizontal counter corresponds to one of 500 segments of each horizontal line.

In the CONSTRUCT mode of operation with S_2 in position 4, the position counters of the PROCESSOR count continuously commencing at the beginning of each sweep of the DISPLAY until a point is indicated by the LIGHT PEN. When a signal is received from the output of the AND gate, the horizontal and vertical position counters of the PROCESSOR stop, the contents therein representing the horizontal and vertical of the LIGHT PEN. A POINT STORED indicator then lights indicating that a point has been stored.

The PROCESSOR contains two horizontal and two vertical counters, one pair being used to store the coordinates of POINT 1, the other pair being used to store the coordinates of POINT 2 in the same manner described above.

In the LINE mode of operation the digital signals from the horizontal and vertical counters are converted to analog voltages in the

hybrid section of the PROCESSOR. These voltages are used to determine the length, slope and position of the line on the DISPLAY. The line is generated as a Lissajous pattern in the DISPLAY MEMORY with sinusoidal deflection signals. The 10 KHz sinusoidal oscillator which generates these signals is shown in Figure 2.1. When the EXECUTE CONSTRUCT button is depressed, S_3 switches from the normal deflection signal to the deflection signal arriving from the hybrid section of the PROCESSOR. S_1 is closed at the same time which allows the line to be written in the DISPLAY MEMORY, and subsequently the line appears on the DISPLAY.

The same basic sequence of events occurs in the CIRCLE mode of operation as in the LINE mode except that a radius counter is employed. This counter stores the magnitude of the radius in bit form which is then coverted to an analog voltage in the hybrid section of the PROCESSOR.

Translation of lines and circles and the construction of concentric circles is accomplished by resetting the appropriate counter(s), thus changing the corresponding analog voltages in the PROCESSOR. In the case of translating a line, for example, this amounts to shifting the DC levels of the Lissajous pattern in the DISPLAY MEMORY.

3.0 Subsystem Operation

3.1 DISPLAY

3.1.1 MONITOR

The ARTRIX DISPLAY system consists of a standard 23" black and white television MONITOR, a LIGHT PEN and a set of CONTROL SWITCHES. These are all located in the DISPLAY CONSOLE as shown in Figure 3.1.

The MONITOR displays the video output of the MEMORY CONTROL UNIT. This video output consists of the contents of both the DISPLAY MEMORY and the POINT MEMORY as explained in Section 3.2.2.2.4. Thus the operator is presented with a continuous view of the contents of the two memories with which he works.

3.1.2 LIGHT PEN

The LIGHT PEN detects the light produced by the scanning of the electron beam in the MONITOR (See Figure 3.2). Because the LIGHT PEN cannot detect light where none is present, the use of this type of light pen necessitates a gray background level on the MONITOR. Thus the MONITOR picture consists of white writing on a gray background. The LIGHT PEN contains an ENABLE button as well as the photo diode light detector and amplifier. The output of the LIGHT PEN amplifier is sent to a line driver in the PEN EMITTER FOLLOWER chassis located in the DISPLAY CONSOLE (Figure 3.1). The ENABLE button controls the output of the LIGHT PEN in such a way that the LIGHT PEN output pulse is ineffective except when the ENABLE button is depressed. This control takes place in the MEMORY CONTROL UNIT. The LIGHT PEN mode switches determine the function of the LIGHT PEN pulse when the ENABLE button is depressed. This control takes place in the MEMORY CONTROL UNIT. The LIGHT PEN mode switches determine the function of the LIGHT PEN pulse when the ENABLE button is depressed (Figure 3.1).

Figure 3.1 DISPLAY CONSOLE

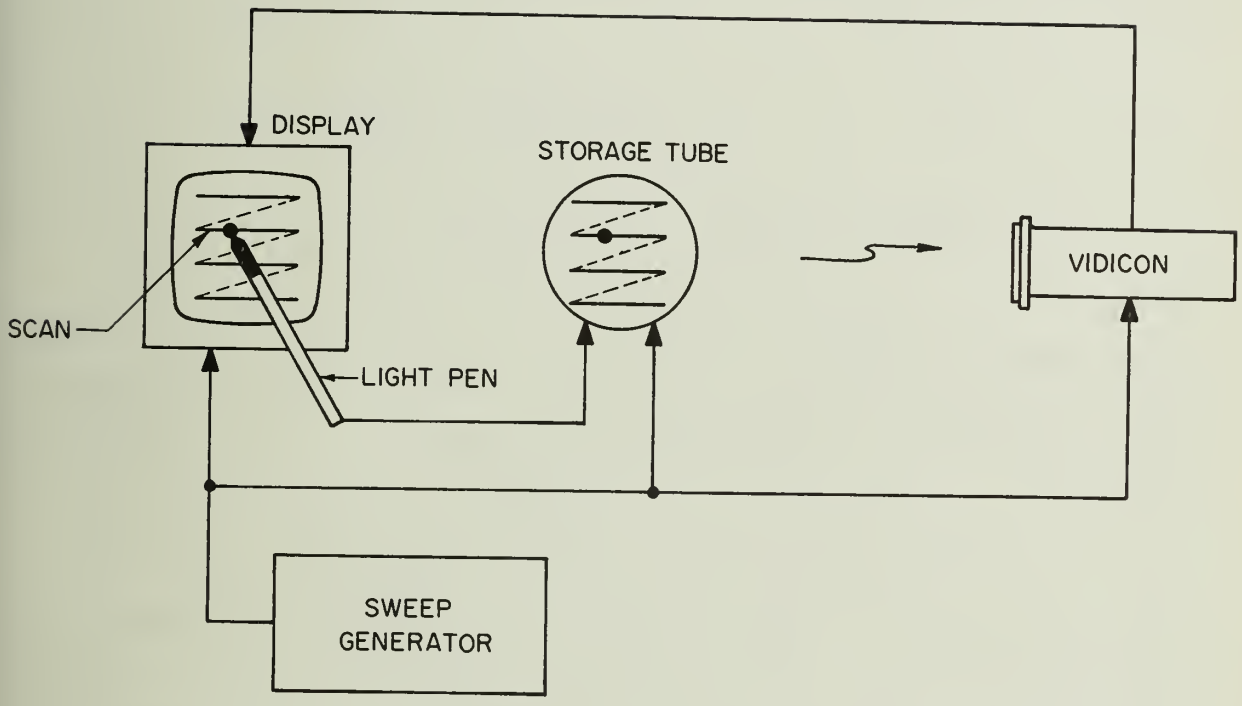


Figure 3.2 Basic ARTRIX Writing Scheme

3.1.3 Control Switches and Indicators

The LIGHT PEN mode section of the CONTROL SWITCHES allows operation of the LIGHT PEN in one of five different mutually exclusive modes: WRITE POINT, WRITE DISPLAY, CONSTRUCT, ERASE DISPLAY, and ERASE POINT. In the WRITE POINT mode, the LIGHT PEN can write one point per television frame into the POINT MEMORY. The WRITE POINT mode switch also causes the WRITE POINT INDICATOR to light. In the WRITE DISPLAY mode the LIGHT PEN can write one point per television frame into the DISPLAY MEMORY. The WRITE DISPLAY mode switch causes the WRITE DISPLAY INDICATOR to light. In either the ERASE POINT or ERASE DISPLAY mode, the LIGHT PEN can write one point per television frame into the ERASE MEMORY. The ERASE POINT and ERASE DISPLAY mode switches cause their respective indicators to light. Information written into the ERASE MEMORY shows up on the MONITOR as a dark shade of gray. This occurs because the output of the ERASE MEMORY is used to delete information from either the POINT MEMORY or the DISPLAY MEMORY video signal depending on whether the ERASE POINT or ERASE DISPLAY mode has been chosen. This is accomplished by blacking the appropriate video signal (POINT or DISPLAY) at points corresponding to those written in the ERASE MEMORY. A description of this operation is given in Section 3.2.2.2.1.2. In the remaining mode, CONSTRUCT, the LIGHT PEN is used to locate points on the MONITOR which are stored in the POINT MEMORY. The actual processing of the LIGHT PEN pulse is accomplished in the MEMORY CONTROL UNIT and a description of these operations is contained in Section 3.2.2.2.3. The CONSTRUCT INDICATOR lights either yellow (LINE) or blue (ARC-CIRCLE) depending on the PROCESSOR mode switches.

The remaining CONTROL SWITCHES can be divided into two groups: the MEMORY erase control switches and the PROCESSOR control switches. There are six switches which control the erase functions of the system: TOTAL, TEMPORARY, POINT, DISPLAY, ERASE, and EXECUTE ERASE (See Figure 3.1).

Five of these six switches have no associated indicators. Depressing the TOTAL button erases all information on all four memories.

Depressing the ERASE, DISPLAY, POINT, or TEMPORARY buttons causes all information in the ERASE MEMORY, DISPLAY MEMORY, POINT MEMORY, or TEMPORARY MEMORY, respectively, to be erased. The EXECUTE ERASE button functions only in either the ERASE POINT mode or ERASE DISPLAY mode. When this button is depressed a sequential process takes place in the MEMORY CONTROL UNIT which accomplishes the following:

1) The contents of the memory (either POINT MEMORY or DISPLAY MEMORY depending on whether the mode is ERASE POINT or ERASE DISPLAY) has its contents blacked out at points corresponding to the contents of the ERASE MEMORY while it is written into the TEMPORARY MEMORY.

2) The original memory (POINT or DISPLAY) and the ERASE MEMORY are completely erased.

3) The information in the TEMPORARY MEMORY is written back into the original memory (POINT or DISPLAY).

4) The TEMPORARY MEMORY is completely erased.

Thus at the end of this process the original memory contains the information that it originally possessed less that information which had appeared in the ERASE MEMORY. During this sequential operation, the EXECUTE ERASE indicator lights.

The remaining set of switches, the PROCESSOR CONTROL switches, control the mode of operation of the PROCESSOR and the contents of the PROCESSOR POINT REGISTERS. There are three mutually exclusive mode switches: LINE, CIRCLE, and ARC. These switches determine whether the PROCESSOR will calculate a circle, a line, or an arc. In each case the appropriate PROCESSOR MODE INDICATOR lights. In order for the PROCESSOR to generate any of these, the LIGHT PEN must be in the CONSTRUCT mode. With the LIGHT PEN in the CONSTRUCT mode, it can be used to designate points on the MONITOR. The first point designated is known as POINT 1 and the second point designated is known as POINT 2. When a point is stored in the PROCESSOR, the appropiate POINT STORED indicator lights. In the CIRCLE mode, POINT 1 is interpreted by the PROCESSOR as the center of the desired circle and POINT 2 is interpreted

as a point defining the circumference of the circle. The radius of the circle is calculated from these two points. When the radius is stored the RADIUS STORED INDICATOR lights. Similarly in the LINE mode, POINT 1 and POINT 2 define the ends of the line for the PROCESSOR. In the CIRCLE mode either POINT 1 or POINT 2 (center or radius) may be changed independently by operating the appropriate reset button (POINT 1 RESET or POINT 2 RESET) and then indicating the new point. When it desired to change the radius of the circle, the RADIUS RESET button must also be depressed. In the LINE mode, a line may be translated by changing POINT 1 as above. Changing POINT 2 in the line mode has no useful significance. The ARC mode has not been implemented in the current system.

There are two buttons remaining: PROCESSOR RESET and EXECUTE CONSTRUCTION. The PROCESSOR RESET button causes the POINT 1, POINT 2, and RADIUS REGISTERS all to be reset simultaneously. With all registers reset, the PROCESSOR RESET INDICATOR lights. The EXECUTE CONSTRUCTION button causes the MEMORY CONTROL unit to write the construction (line or circle) into the DISPLAY MEMORY. The EXECUTE CONSTRUCTION READY INDICATOR lights when the PROCESSOR is in a state such that a construction has been generated and can be written into the DISPLAY MEMORY at the option of the operator.

The CONTROL SWITCHES and INDICATORS are connected to the MAIN CONSOLE through the DISPLAY CONSOLE JUNCTION BOX, Figure 3.3). This junction box serves as a distribution point for power and control signals in the DISPLAY CONSOLE. It contains two printed circuit cards, a LAMP DRIVER card and a SWITCH FILTER card. The LAMP DRIVER card drives the CONTROL SWITCH INDICATORS which operate from logic level signals generated in the PROCESSOR and MEMORY CONTROL UNIT. Other indicators are operated directly by the CONTROL SWITCHES. The FILTER card in conjunction with the clamping diodes which are mounted externally to the card serves to generate low impedence logic signals from the CONTROL SWITCHES in order to drive the logic circuits in the MAIN CONSOLE.

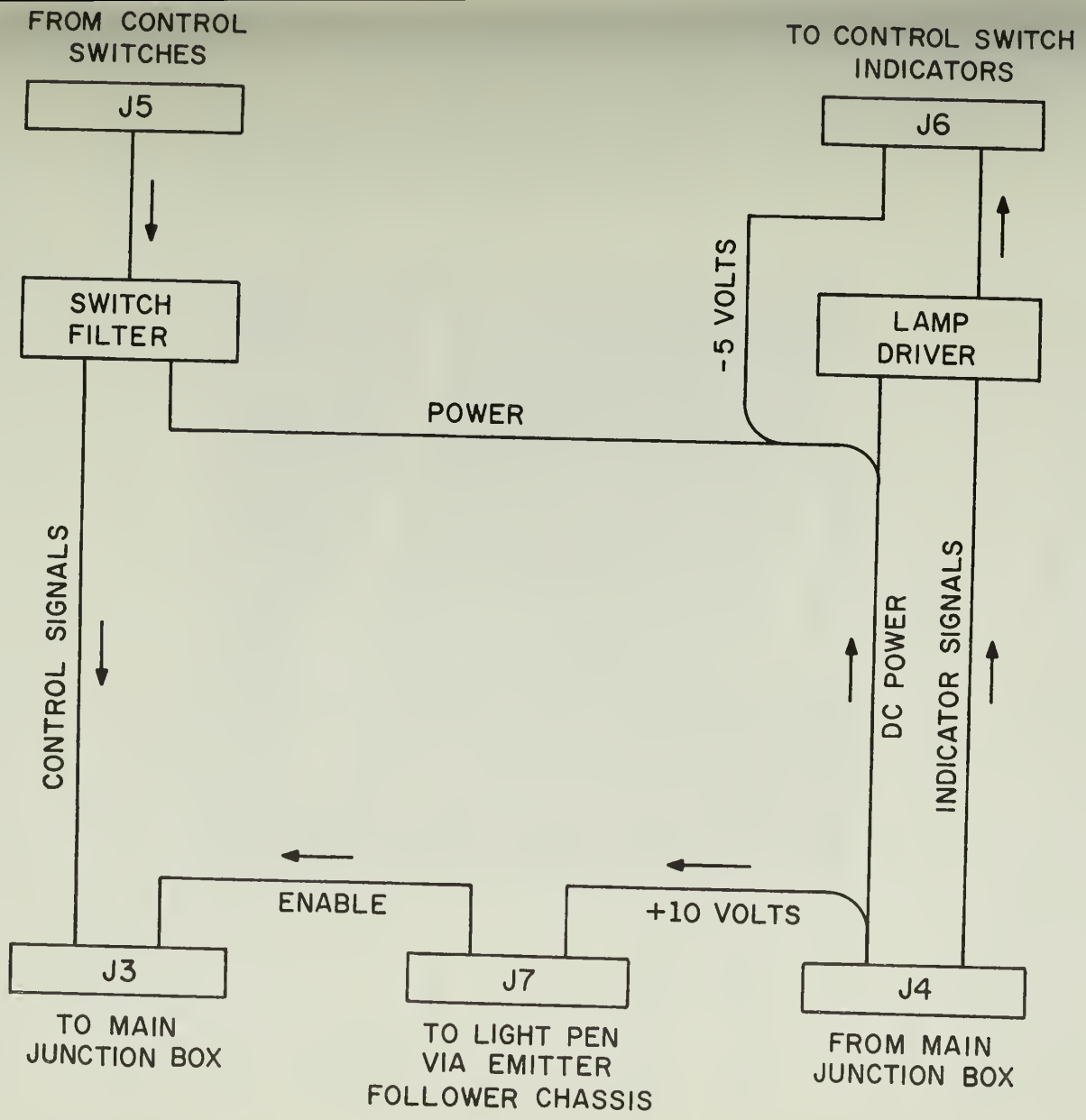


Figure 3.3 Simplified Schematic of DISPLAY CONSOLE JUNCTION BOX

Both the returning ENABLE signal and the power for the LIGHT PEN pass through connector J7.

Connectors J3 and J4 carry control signals and DC power between the DISPLAY CONSOLE and the MAIN CONSOLE. Connectors J5 and J6 carry control signals between the CONTROL SWITCHES and the DISPLAY CONSOLE JUNCTION BOX.

3.2 Memory

3.2.1 Memotron - Vidicon Storage Cell

3.2.1.1 Memotron Storage Units

As mentioned previously the MEMORY of ARTRIX consists of four MEMOTRON-VIDICON units. See Figure 3.4. The MEMOTRON storage tube serves as the storage medium and the VIDICON television camera as the readout mechanism. Since all four memory units are identical, a brief description of a typical MEMOTRON-VIDICON unit will be given in this report. A thorough explanation of the operation of the MEMOTRON unit is contained in the INSTRUCTION MANUAL for MEMO-CORDER STORAGE UNIT, MODEL 106, available from HUGHES AIRCRAFT COMPANY, VACUUM TUBE PRODUCTS DIVISION, OCEANSIDE, CALIFORNA. Similarly a complete explanation of the VIDICON television camera system is contained in TECHNICAL MANUALS CODE Nos. 6X-330 (3000 SERIES HIGH RESOLUTION TELEVISION CAMERAS), 6X-331(A) (3900 SERIES HIGH RESOLUTION CLOSED CIRCUIT TELEVISION CAMERA CONTROLS) and 6X-337 (PLUG-IN SYNCHRONIZATION GENERATORS), all of which are available from COHU ELECTRONICS, INC., KINTEL DIVISION, BOX 623, SAN DIEGO, CALIFORNIA, 92112.

The MEMOTRON unit is a Hughes Aircraft MEMO-CORDER MULTIFUNCTION STORAGE UNIT MODEL 106. It consists of a Hughes MEMOTRON storage tube along with all the associated circuitry except x, y, z, and erase input signals. In ARTRIX the x and y signals are generated in the MEMORY CONTROL UNIT. These are linear sawtooth deflection voltages occurring at the standard television frequencies of 60 Hertz vertically and 15,750 Hertz horizontally. An exception to this occurs at

Figure 3.4 Typical Memotron-Vidicon Combination

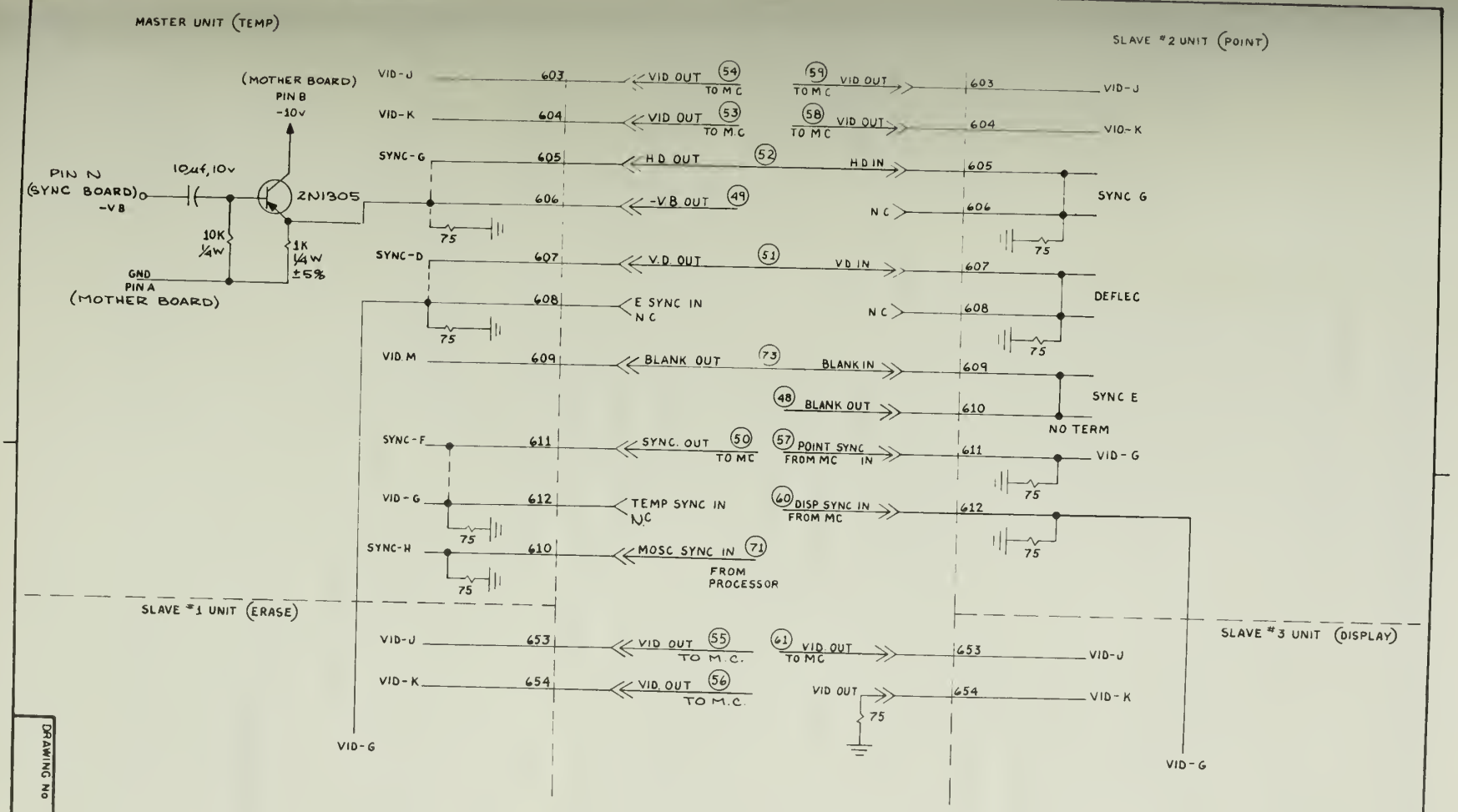
the DISPLAY MEMORY when ARTRIX is in the CONSTRUCT mode, in which case the x and y signals are the Lissajous deflection voltages from the PROCESSOR. Two z-input signals are required: a gate signal which serves to unblank the writing beam and a z-axis signal which modulates the beam. The gate signal is derived from the television blanking signal. An exception to this occurs at the DISPLAY MEMORY when ARTRIX is in the CONSTRUCT mode. In this case the gate signal is generated from the average magnitude of the Lissajous deflection signals. In this manner the writing beam intensity is reduced when small patterns are being written. The z-axis signal is generated by a Z-AXIS DRIVER circuit whose input may be shaped video, pen pulses, or a d.c. voltage level. The erase inputs are controlled by the erase relays in the MEMORY CONTROL UNIT.

3.2.1.2 Vidicon Cameras

Any pattern written onto the storage surface of the MEMOTRON shows up on the face of the tube. This pattern is imaged on a VIDICON type closed circuit television camera. The signal generated at the camera is sent to the CAMERA CONTROL UNIT. There are four camera heads and four camera control units in ARTRIX. One control unit contains a synchronization generator which generates standard EIA synchronization, drive, and blanking for the DISPLAY MEMORY and MEMORY CONTROL UNIT. This synchronization generator is itself synchronized to the master oscillator located in the PROCESSOR. Figure 3.5 is a partial schematic of the CAMERA CONTROL UNITS showing the modifications required by ARTRIX. This figure also shows the interconnections between units.

Note that the MASTER and SLAVE #1 units are in a common chassis as are SLAVE #2 and #3 units. Horizontal drive, vertical drive and blanking signals are supplied to both control units within the chassis from a common input.

The 2N1305 transistor is an emitter follower which buffers the vertical blanking pulse going to J606 of the MASTER UNIT. These vertical blanking pulses go to the MEMORY CONTROL UNIT where, after level shifting, they are sent to the PROCESSOR and used to distinguish even and odd fields of the video frame. This is explained in



NOTES

3. VID-J = VIDEO PLUG-IN CIRCUIT BOARD, PIN J.
2. M.C. = MEMORY CONTROL UNIT.
1. DOTTED LINES INDICATE CONNECTIONS WHICH HAVE BEEN REMOVED

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DEPARTMENT of COMPUTER SCIENCE
University of Illinois, Urbana, Illinois

PROJECT ARTRIX

TITLE PARTIAL SCHEMATIC SHOWING MODIFICATIONS TO COHU CAMERA CONTROL UNITS

FOR W.J. KUBITZ DRAWN BY M. MILLER

DATE DRAWN 8-4-66 DATE SIGNED

APPROVED BY

Figure 3.5 Partial Schematic of CAMERA CONTROL Unit

Section 3.3.1.1. The horizontal drive pulses originate in the MASTER UNIT and are fed to Slaves #2 and #3 through CABLE 52. Likewise, the vertical drive pulses are sent through CABLE 51. Composite blanking originates at connector J609 of the MASTER UNIT and goes to connector J609 of the Slave units on CABLE 73. Since connectors J609 and J610 of the slave UNIT are common terminals, blanking appears at J610 where it is fed to the MEMORY CONTROL UNIT on CABLE 48. Composite synchronization appears at connector J611 of the MASTER UNIT, and goes to the MEMORY CONTROL UNIT on CABLE 50. The synchronization pulses from the PROCESSOR are fed to the CAMERA CONTROL UNIT OSCILLATOR at connector J610 of the MASTER UNIT. Connectors J603 and J604 of the MASTER UNIT are the video outputs of the TEMPORARY MEMORY. Connectors J653 and J654 of the SLAVE #1 UNIT are the video outputs of the ERASE MEMORY. Similarly, connectors J603 and J604 of SLAVE #2 unit correspond to the POINT MEMORY video and connectors J653 and J654 of SLAVE #3 unit correspond to DISPLAY MEMORY video. There is no connection to connectors J606 and J608 of the SLAVE #2 UNIT, since these are drive pulse outputs and are not used. The remaining four connectors are synchronization input connectors. No synchronization is added to the video signal in the CAMERA CONTROL UNITS, thus the TEMPORARY synchronization (MASTER) and ERASE synchronization (SLAVE #1) inputs are not used. The POINT (SLAVE #2) and DISPLAY (SLAVE #3) synchronization inputs are used, however, but not for synchronization. These inputs are used in the ERASE mode. In this mode a signal is applied to the synchronization input which causes the video level to be reduced to the black level, thus "erasing" a portion of the video signal. By adjusting the synchronization level potentiometer in the control units, the input signal reduces the video level only to the black level rather than to some negative level.

3.2.2 MEMORY CONTROL UNIT

3.2.2.1 Synchronization, Blanking and Deflection Circuits

3.2.2.1.1 Synchronization Circuits

A standard composite EIA synchronization signal is supplied to the MEMORY CONTROL UNIT from the CAMERA CONTROL UNIT at connector J50 (see Figure 3.6). The CAMERA CONTROL also supplies this synchronization signal to the PROCESSOR (see Section 3.3.1.1). This signal is fed to the VIDEO ADDER on card A8 and to the SYNCHRONIZATION SEPARATOR circuit on card C1. At the VIDEO ADDER card, the composite synchronization signal is added to the output video signal being sent to the DISPLAY CONSOLE. At the SYNCHRONIZATION SEPARATOR, the synchronization signal is separated into horizontal and vertical synchronization pulses. The horizontal synchronization pulses are then passed to the HORIZONTAL RAMP GENERATOR circuit on card C3, where they are used to synchronize the horizontal sawtooth deflection voltage. The vertical synchronization pulses are fed to the VERTICAL RAMP GENERATOR on card C2, where they are used to synchronize the vertical deflection voltage. The vertical synchronization pulses are also sent to the VERTICAL SYNCHRONIZATION LOGIC DRIVER (also on C1), where the synchronization pulses are converted to logical signal levels compatible with the logic circuits. The use of these VERTICAL SYNCHRONIZATION LOGIC PULSES will be described later when the erase operation is discussed.

3.2.2.1.2 Deflection Circuits

The horizontal and vertical deflection signals generated by the circuits on cards C2 and C3 are sent directly to the POINT, ERASE and TEMPORARY MEMORIES at connectors J62 and J64. These ramps also pass through the DEFLECTION CONTROL RELAY (on card C4) and to the DISPLAY MEMORY at connectors J38 and J39 except when the LIGHT PEN is in the CONSTRUCT mode and the PROCESSOR is in the EXECUTE CONSTRUCTION READY state. The logical AND of these two conditions is accomplished on card B5. If the LIGHT PEN is in the CONSTRUCT mode and the PROCESSOR

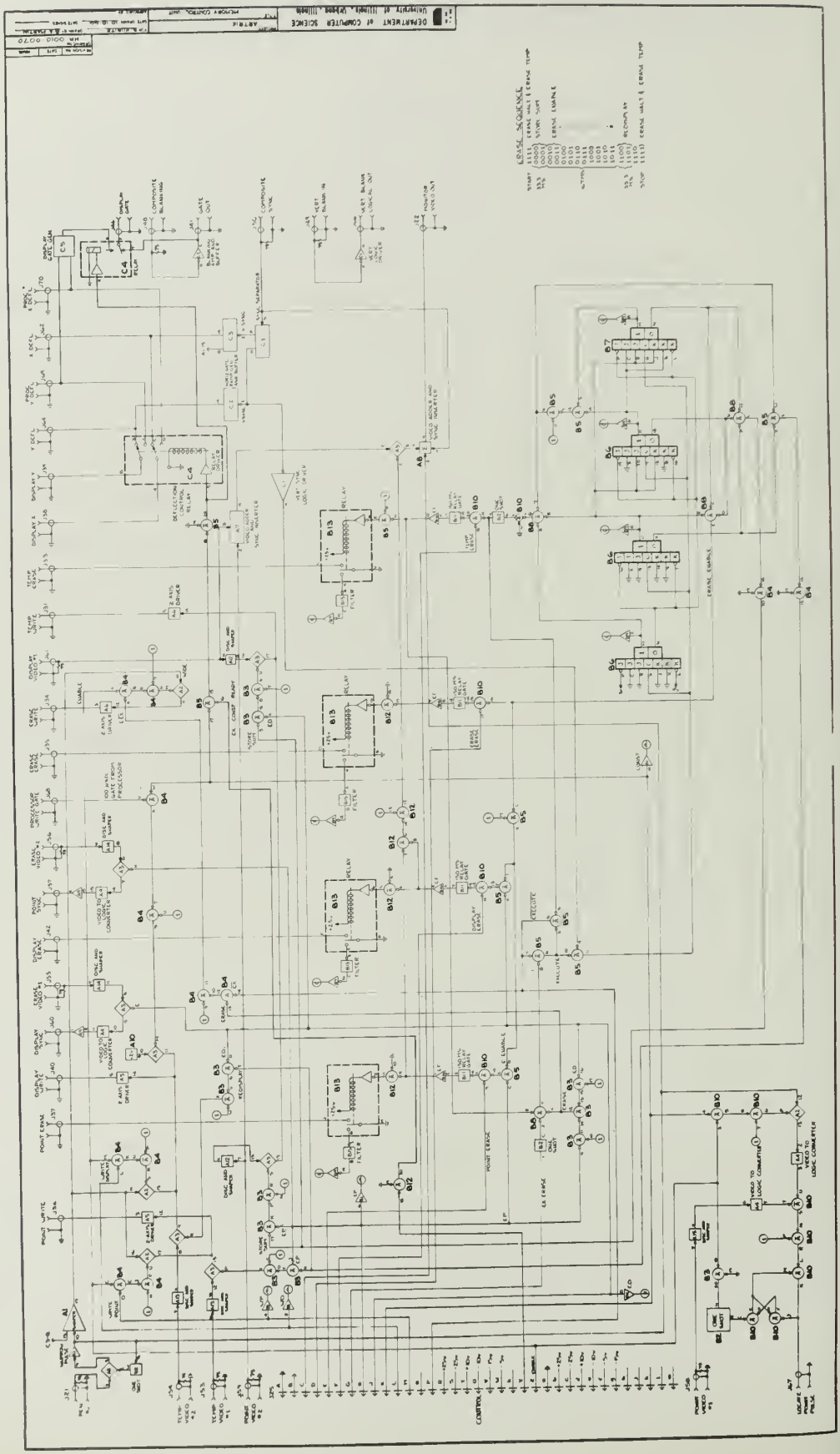


Figure 3.6 MEMORY CONTROL Unit

is in the EXECUTE CONSTRUCTION READY state the DEFLECTION CONTROL RELAY is energized and the DISPLAY MEMORY deflection inputs at connectors J38 and J39 are connected to the PROCESSOR deflection outputs (connectors J70 and J69). Under these circumstances, the deflection of the write beam in the DISPLAY MEMORY is controlled by the PROCESSOR.

Note that C3, the HORIZONTAL RAMP GENERATOR card has one other input (see Figure 3.6). This input is used when the LIGHT PEN is in a WRITE or ERASE mode. It causes the horizontal deflection voltage to pause for the duration of the LIGHT PEN pulse, thus producing no motion of the writing beam at this time. An explanation of this operation is discussed in Section 3.2.2.1.3.

3.2.2.1.3 Blanking and Gating Circuits

Composite EIA blanking is supplied to the MEMORY CONTROL UNIT at connector J48. This signal is applied to the BLANKING AMPLIFIER and BUFFER circuit on card C1. This circuit changes the level of the BLANKING signal to the level required by the GATE input of the MEMO-CORDER storage units. The GATE input of the storage units is used to unblank the writing beam during each horizontal trace. This unblanking signal appears at connector J41 and drives the POINT, ERASE and TEMPORARY MEMORY gate inputs. The gate input of the DISPLAY MEMORY normally receives its unblanking signal through the DISPLAY GATE CONTROL RELAY oncard C4. This is the same gate signal as that supplied to the other memories. However, when the LIGHT PEN is in the CONSTRUCT mode and the processor is in the EXECUTE CONSTRUCT READY state, the GATE CONTROL RELAY is energized and the gating signal for the DISPLAY MEMORY is obtained from the DISPLAY GATE GENERATOR circuit on card C5. The DISPLAY GATE GENERATOR circuit develops an unblanking voltage output which depends on the magnitude of the deflection signals from the PROCESSOR. In this way, the writing beam intensity in the DISPLAY MEMORY is reduced as the magnitude of the deflection signal from the PROCESSOR decreases. The reduction of the beam velocity which accompanies a decrease in pattern

size at fixed frequency necessitates this lower beam intensity. If the beam intensity is not reduced, small patterns will be smeared.

A vertical blanking pulse is supplied to the MEMORY CONTROL UNIT from the CAMERA CONTROL UNIT at connector J49. This signal is applied to the VERTICAL BLANKING LOGIC DRIVER circuit (also on card C1).. Here it is changed to system logic levels and sent to connector J66 to supply the PROCESSOR with pulses at television field rates. See Section 3.3.1.1 for an explanation of the use of this signal.

3.2.2.2 Logic and Video Circuits

3.2.2.2.1 ERASE Modes

3.2.2.2.1.1 TOTAL ERASE Functions

Complete erasure of any one or all of the four memory storage units is accomplished through operation of the appropriate button on the DISPLAY CONSOLE. Selective erasure of the POINT and DISPLAY MEMORIES is possible and is described in Sections 3.2.2.2.1.2, 3.2.2.2.1.3 and 3.2.2.2.1.4.

For complete erasure of the POINT, DISPLAY, ERASE or TEMPORARY MEMORY, the operator depresses the POINT, DISPLAY, ERASE or TEMPORARY erase button on the DISPLAY CONSOLE. This generates a logic signal in the DISPLAY CONSOLE JUNCTION BOX (Figure 3.7) which is sent to the MAIN CONSOLE and the MEMORY CONTROL UNIT through the interconnecting cables and the MAIN CONSOLE JUNCTION BOX (Figure 3.8). These signals appear at connector J25 of the MEMORY CONTROL UNIT on pins C, D, E, and F. Complete erasure of the POINT MEMORY will be described as typical of the four memories. In the following discussion, refer to Figure 3.9. The logic signal generated at the DISPLAY CONSOLE JUNCTION BOX appears at connector J25, Pin E. This logic signal is sent to a NAND circuit on card B10 which is used as an OR circuit. Thus a logical zero at either pin 9 or pin 10 of card B10 causes the 150 millisecond RELAY GATE circuit on card B11 to be triggered. This

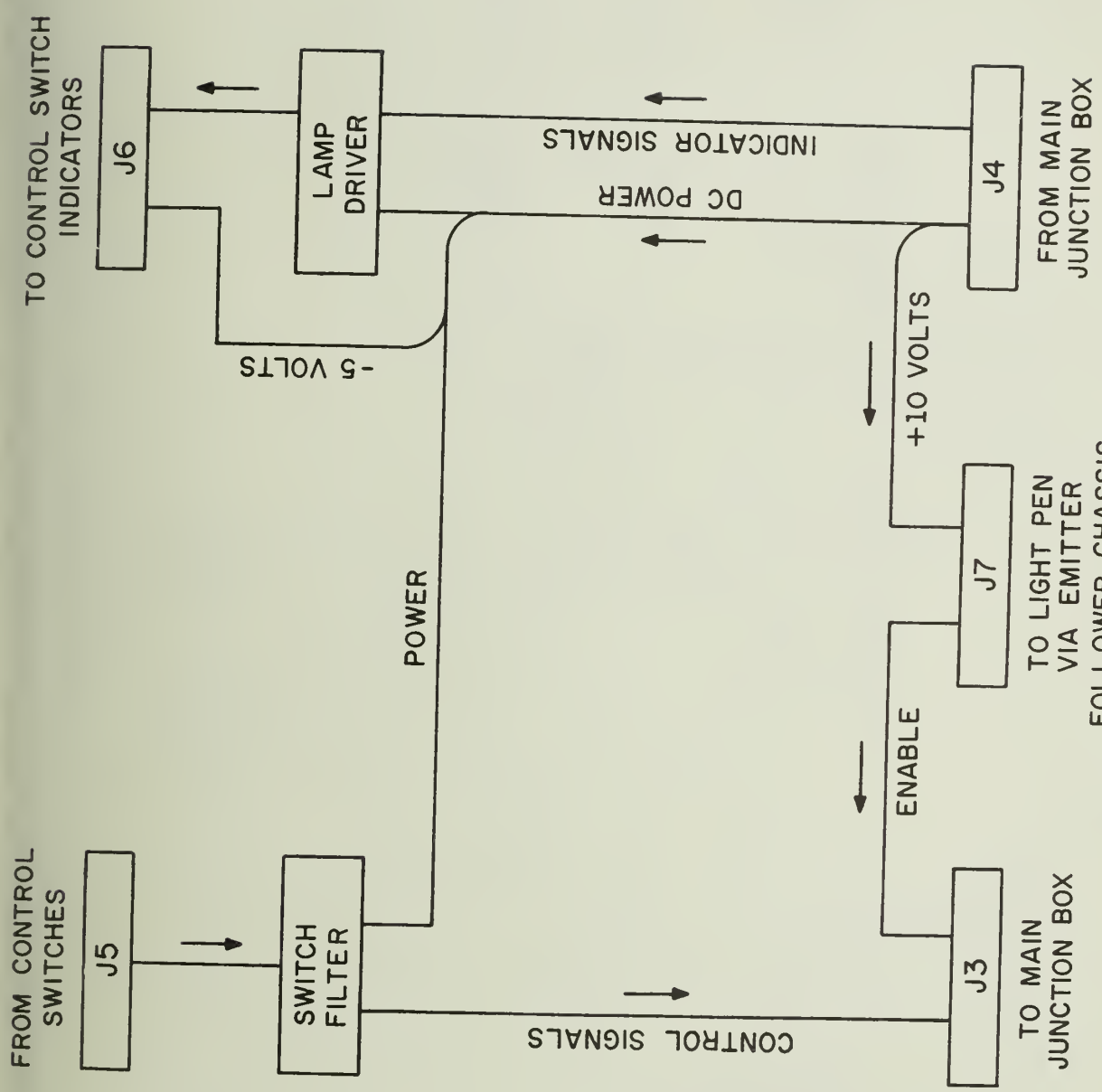


Figure 3.7 Simplified Diagram of DISPLAY CONSOLE JUNCTION BOX

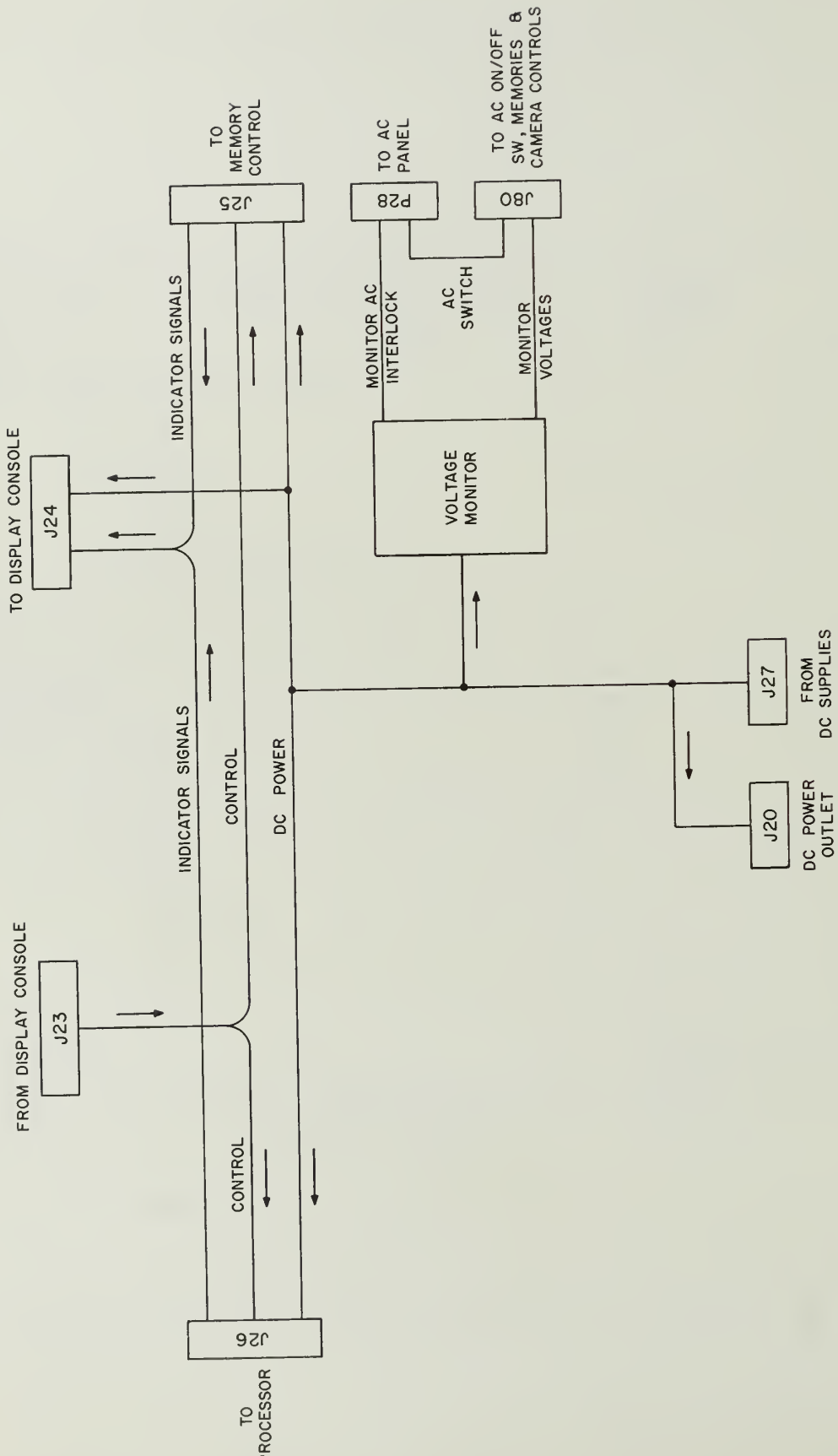


Figure 3.8 Simplified Diagram of Main JUNCTION BOX

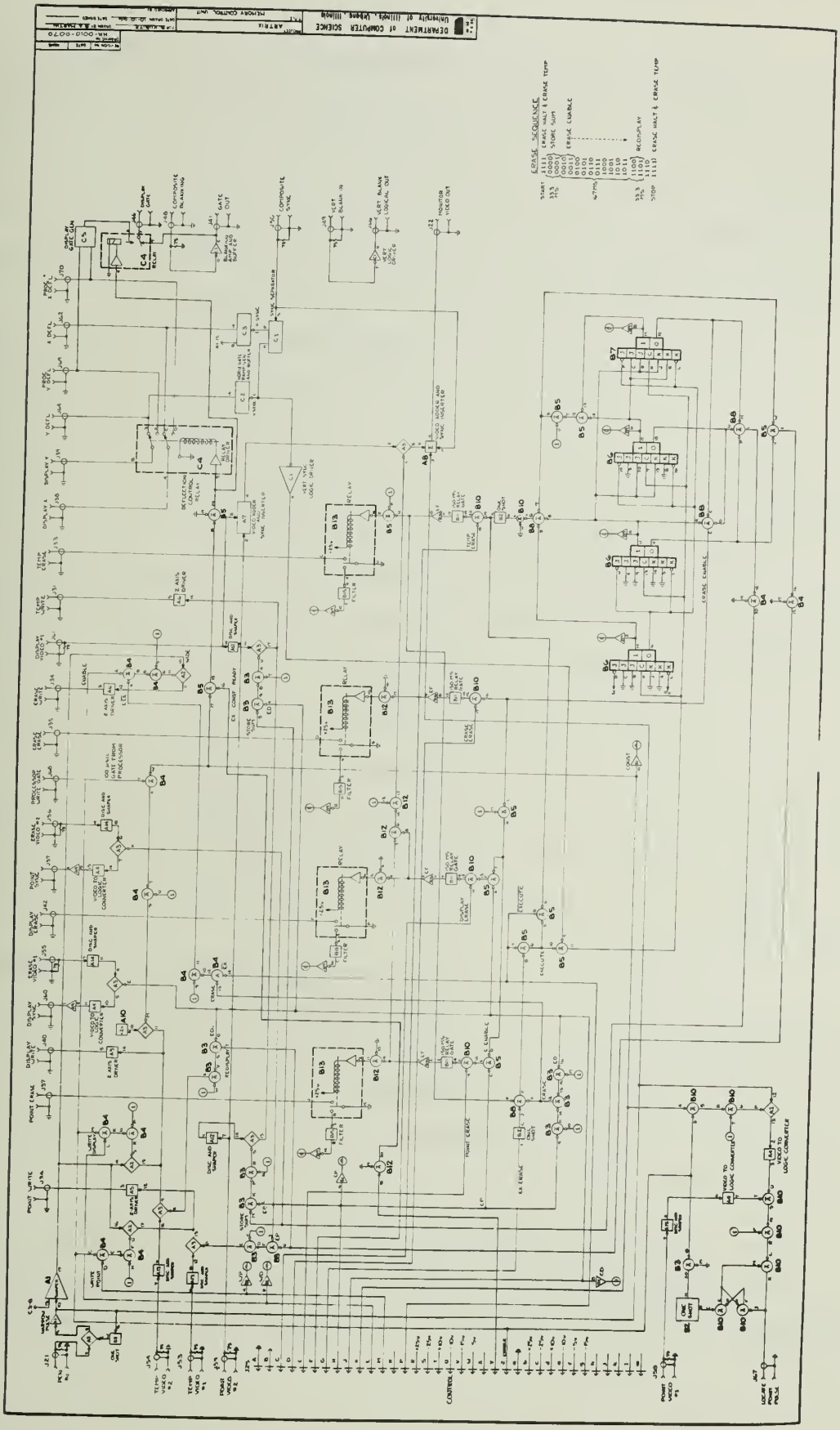


Figure 3.9 Schematic of MEMORY CONTROL UNIT

circuit is buffered by an emitter follower on card B16 and causes a relay on card B13 to be energized for 150 milliseconds. The NAND circuit on B12 is an inverter for the relay driver. The contacts of the relay ground the erase input of the storage unit. This causes the potential in the storage tube to be changed such that its storage surface is erased. An explanation of this operation may be found in the instruction manual for the HUGHES MEMO-CORDER Multifunction Storage Unit Model 106.

When the normally closed closed contact of the erase relay opens, the POINT ERASE indicator on card B9 lights. The erase circuitry for the other memories is essentially the same as that for the POINT MEMORY. The purpose of the other input on card B10 (pin 10) will be discussed when the EXECUTE ERASE sequence is explained in Section 3.2.2.2.1.4. Note that the output of card B16 pin 1 and card B16 pin 4 also go to card B12, pins 7 and 8. Again card B12 acts as an OR circuit and opens the analog gate on card A3 when an erasure is occuring in either the POINT or DISPLAY MEMORY. This gate interrupts the video signal to the display during the 150 millisecond erase period.

The output of card B16, pin 10, also serves a dual purpose. In addition to triggering the TEMPORARY ERASE RELAY on card B13, the signal helps prevent the re-initiation of an EXECUTE ERASE cycle until any current cycle has been completed. This is accomplished at card B8, pin K. This will be explained in more detail when the EXECUTE ERASE cycle is discussed.

It is possible to erase all memories completely by operating the TOTAL ERASE button on the DISPLAY CONSOLE. This is accomplished by simultaneously erasing the individual memories. Operation of the TOTAL ERASE button causes logic signals to be applied to all four erase circuits. These logic signals are generated in the DISPLAY CONSOLE JUNCTION BOX.

3.2.2.2.1.2 The ERASE POINT Pen Mode

The mode of operation of the pen is determined by the CONTROL SWITCHES on the DISPLAY CONSOLE. In the ERASE POINT mode a logic signal

is generated in the DISPLAY CONSOLE JUNCTION BOX which is sent to the MEMORY CONTROL UNIT on J25, pin H. This signal causes the ERASE POINT indicator in the MEMORY CONTROL to turn off (the light which is out indicates the mode). In addition, this signal goes to a NAND circuit on card B3 (after inversion), where it is ORed with the ERASE DISPLAY signal. The output of this NAND is called the ERASE signal and indicates that the system is in the ERASE mode (either ERASE POINT or ERASE DISPLAY). The ERASE POINT signal goes to a NAND circuit on card B5 where it is NANDed with the ERASE ENABLE signal. This will be explained when the EXECUTE ERASE operation is discussed. The ERASE POINT signal also goes to NAND circuits on card B3, pins J and L. At pin J it is NANDed with the REDISPLAY signal and at PIN L it is NANDed with the STORE SUM signal. Both signals are used in the EXECUTE ERASE operation and will be discussed later. The remaining location to which the ERASE POINT signal is sent is the video gate on card A3, pin H. This signal causes the gate to open, thereby allowing the video from the ERASE MEMORY to pass from the DISCRIMINATION and SHAPING circuit (card A14) to the VIDEO-TO-LOGIC CONVERTER circuit. From there it passes through the buffer circuit on card A9 to the synchronization input of the POINT CAMERA CONTROL UNIT. This occurs for the following reason: In the ERASE mode (ERASE POINT or ERASE DISPLAY) the pen writes into the ERASE MEMORY. The information in the ERASE MEMORY is to be removed subsequently from either the DISPLAY MEMORY or the POINT MEMORY (depending on the mode). To accomplish this the video output of the memory (in this case the output of the POINT MEMORY) is fed through a discriminator and shaper circuit. The purpose of this circuit is threefold: to strip the blanking from the video; to establish the threshold separating erase information from noise; and to standardize the pulse shape of this erase information. This information then passes through the video gate on card A3 to the VIDEO-TO-LOGIC CONVERTER. The purpose of this circuit is to shift the output of the DISCRIMINATION and SHAPING circuit to levels compatible with the synchronization input of the CAMERA CONTROL UNIT

(either POINT or DISPLAY). The signal then passes through a buffer which drives the cable going to the control unit. At the control unit the signal causes the output video to be pulled to the black level whenever erase information occurs. Thus, any video occurring in the POINT MEMORY at a location corresponding to that of erase information in the ERASE MEMORY is deleted from the video output. Note, however, that the information is not actually removed from the POINT MEMORY but is only reduced to the black level at the output.

The function of the ERASE signal will now be explained. Recall that the ERASE signal is generated at card B3, pin 12 by the presence of either the ERASE POINT signal or the ERASE DISPLAY signal. This signal goes to card B8, pin H where it is NANDed with other signals in order to allow operation of the EXECUTE ERASE sequence. This sequence will be explained below. The ERASE signal also goes to the NAND circuit on card B4, pin 13 where it is NANDed with the negation of the ERASE EXECUTION signal. The purpose of this NAND circuit is to prevent the pen from writing into the ERASE MEMORY unless two conditions are met: (1) the pen is in the erase mode, and (2) no erase execution is in progress. If both of these conditions are met, the output of this NAND appears at the input of the NAND circuit on card B4, pin 4, where it is NANDed with the pen ENABLE signal. The pen ENABLE signal is generated in the DISPLAY CONSOLE JUNCTION BOX when the ENABLE BUTTON on the LIGHT PEN is depressed. If the pen ENABLE signal is present along with the signal just mentioned, the gate on card A2, pin M opens. This gate allows the output of the pen SHAPER circuit on card A1 to pass to the Z-AXIS DRIVER circuit on card A6. The output of the Z-AXIS DRIVER appears at the write input of the ERASE MEMORY. Thus, the pen writes into the ERASE MEMORY and the operator can accumulate areas to be erased in this memory. The operation of the pen shaping circuit will be described below in Section 3.2.2.2.2.1. The purpose of the Z-AXIS DRIVER circuit is to shift the video or pen pulse level to a level sufficient to drive the Z-AXIS input of the MEMO-CORDER unit. The

voltage at the MEMO-CORDER Z-AXIS input determines whether the MEMO-CORDER writing beam is on or off.

3.2.2.2.1.3 The ERASE DISPLAY Pen Mode

The ERASE DISPLAY mode is identical to the ERASE POINT mode except that the gate on card A3, pin H does not open, thus preventing the output of the ERASE MEMORY from reducing the POINT MEMORY video to the black level. Instead, the gate on card A3, pin 3 opens and the ERASE MEMORY output is used to reduce the DISPLAY MEMORY video to the black level.

3.2.2.2.1.4 The EXECUTE ERASE Sequence

Recall that even though erase information may have been accumulated in the ERASE MEMORY and that this information may have caused reduction of the POINT or DISPLAY MEMORY video to the black level, no actual erasure has taken place. In order to accomplish actual erasure of selected areas in the POINT or DISPLAY MEMORIES it is necessary to go through an EXECUTE ERASE cycle. This cycle is initiated by a signal generated in the DISPLAY CONSOLE JUNCTION BOX when the EXECUTE ERASE button is depressed. This signal appears at connector J25, pin G and triggers a 2 millisecond multivibrator which sets an R-S flip-flop on card B5, pins 3, 4, 5, 6, 7, and 8. Note that the multivibrator trigger pulse passes through the NAND circuit on card B8, pin J. This NAND circuit will not allow the trigger pulse to pass unless the pen is in the ERASE (POINT or DISPLAY) mode and the TEMPORARY MEMORY is not being erased. The latter will be explained when the erase cycle is described. Assuming that these two conditions are met, the R-S flip-flop will be set. This flip-flop performs three functions. First, the set condition of the flip-flop applies a signal to connector J25, pin P which causes the EXECUTE ERASE indicator to light on the DISPLAY CONSOLE control panel indicating to the operator that the EXECUTE ERASE cycle is being executed. Second, this signal is applied to card B4, pin 14, where it negates the

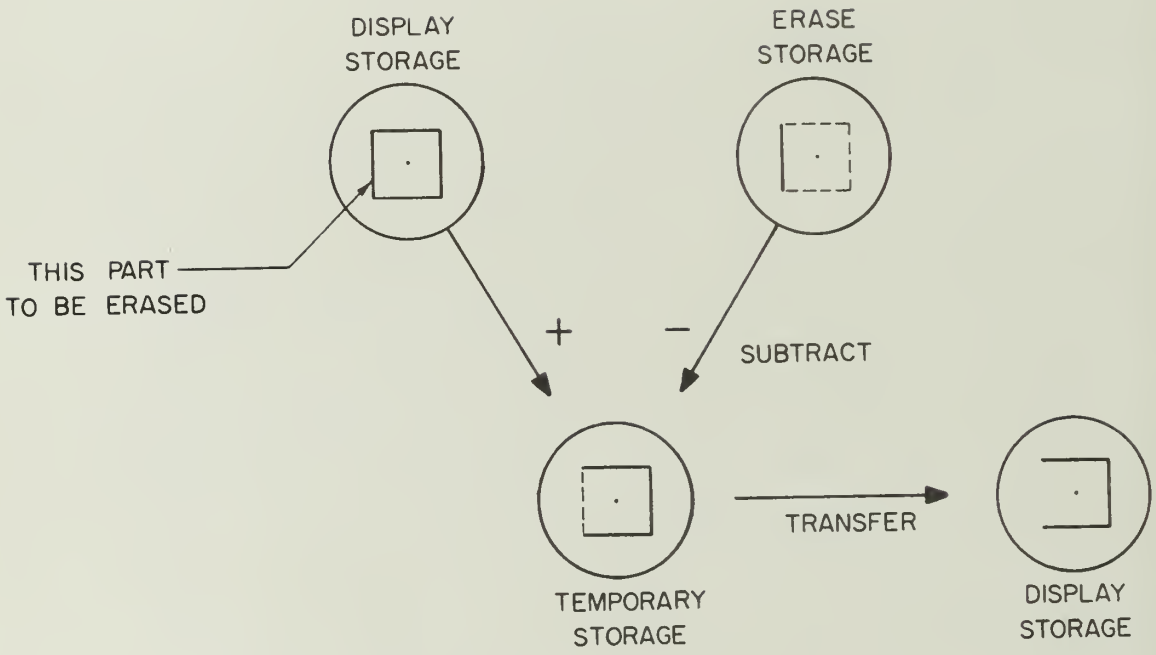


Figure 3.10 a The ERASE Operation

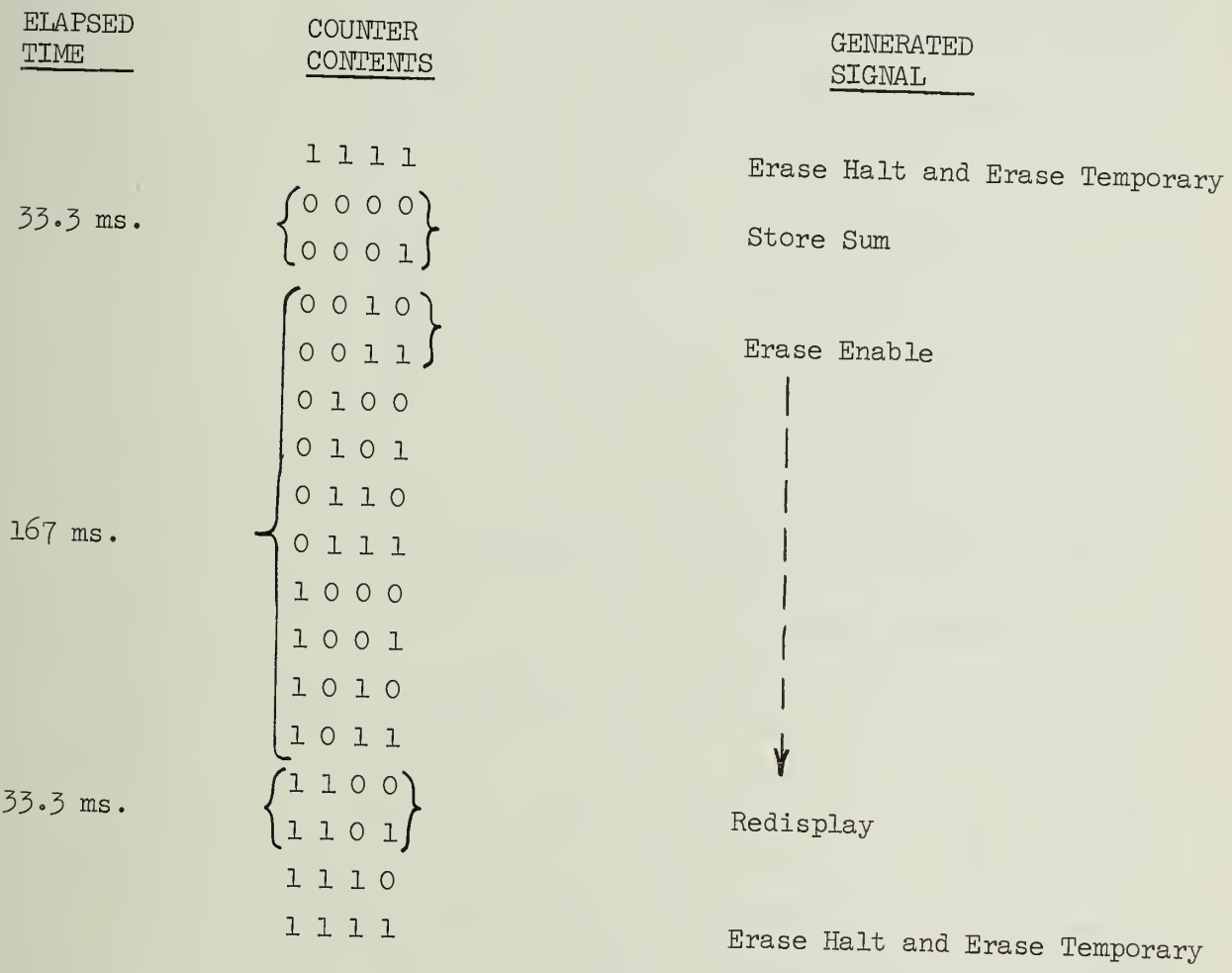


Figure 3.10 b. The EXECUTE ERASE Counter Sequence

output of the NAND circuit thus preventing the pen from writing into the ERASE MEMORY. Third, the reset side of the flip-flop opens the gate on card B5, pin 10 and allows vertical synchronization logic pulses to pass to the 4 bit counter (card B6 and B7). This counter controls the following sequence of operations. The video of the memory being erased is transferred to the TEMPORARY MEMORY. Recall that the output video corresponding to information being erased has been reduced to the black level. The memory being operated on (POINT or DISPLAY) and the ERASE MEMORY are then erased and the information in the TEMPORARY MEMORY is rewritten into the original memory. Finally, the TEMPORARY MEMORY is erased. This sequence is shown in Figure 3.10.

In the 1111 state the counter is in its reset state. When the gate on card B5, pin 11, opens, the counter begins cycling. In the 000X (X = 0 or 1) state the POINT or DISPLAY memory video (certain portions of which have been reduced to the black level) is placed in the TEMPORARY MEMORY. The STORE SUM signal is formed at pins L, M, N, and P on card B8 and is fed to the gates on card B3, pins M and 3. At pin M the STORE SUM signal is NANDed with the ERASE POINT mode signal. The output of this NAND gate opens a gate on card A3, pin 5, allowing video from the POINT MEMORY to be written in the TEMPORARY MEMORY by means of the Z-AXIS DRIVER circuit on card A6, pin 14. The Point video is passed through a DISCRIMINATOR and SHAPER circuit on card A12, pin 7 before passing to the gate. These circuits perform as explained previously. Had the pen been in the ERASE DISPLAY mode rather than in the ERASE POINT mode, the NAND circuit on card B3, pin 3 would have opened a video gate on card A3, pin U, and the video gate on card A3, pin S, would have remained closed. The counter next goes through the 001X states. During these states the ERASE ENABLE signal is generated at card B8, pin E. This signal passes to three NAND circuits. At the NAND circuit on card B10, pin 16 (which behaves like a NOR), the signal triggers a 150 millesecond RELAY GATE circuit on card B11, pin 14, which causes erasure of the ERASE MEMORY as explained in Section 3.2.2.1.1.

At card B5, pin 1, the signal causes the DISPLAY MEMORY to be erased if the pen is in the ERASE DISPLAY mode. On the other hand, if the pen is in the ERASE POINT mode the NAND circuit on card B5, pin D, causes the POINT MEMORY to be erased. Since the erase relays are controlled by the 150 millisecond RELAY GATE circuits, the duration of the erasure process is 150 milliseconds. Thus, during the next 8 states (167 milliseconds) of the erase counter no operation is performed. These states include all 01XX and 10XX states. During the 110X states the REDISPLAY signal is generated at card B5, pin X. This signal goes to a NAND circuit on card B3, pin H where it opens a gate on card A3, pin P, if the pen is in the ERASE POINT mode. This gate allows the video from the TEMPORARY MEMORY, which has already passed through the DISCRIMINATOR AND SHAPER circuit on card A13, pin 14, to pass to the Z-AXIS DRIVER circuit on card A5, pin 12. This circuit writes the information back into the original memory, in this case the POINT MEMORY. In the ERASE DISPLAY mode, the NAND gate on card B3, pin T, the video gate on card A3, pin K, the DISCRIMINATOR AND SHAPER circuit on card A13, pin 7, and the A-AXIS DRIVER on card A5, pin 14 perform a similar function. The 1110 state of the counter performs no function, and the 1111 state generates the STOP signal at the NAND circuit on card B8, pin 6. The STOP signal triggers a 2 millisecond ONE SHOT circuit on card B2, pin 6 which resets the R-S flip-flop on card B5, pins 3 through 8, thus ending the counting cycle. The STOP signal also triggers the TEMPORARY MEMORY 150 millisecond RELAY GATE on card B11, pin 19, causing the TEMPORARY MEMORY to be erased. This is accomplished through the NAND circuit on card B10, pin 19 (used as a NOR). Since the 150 millisecond period required to erase the TEMPORARY MEMORY begins when the counter stops, a re-initiation of the erase cycle is inhibited while the TEMPORARY MEMORY is being erased. This is accomplished when the signal at card B16, pin 10, negates the output of the NAND circuit on card B8, pin K.

3.2.2.2.2 Writing Modes

3.2.2.2.2.1 WRITE POINT Mode

The WRITE POINT mode signal is generated in the DISPLAY CONSOLE JUNCTION BOX when the WRITE POINT pen mode switch is depressed. This signal arrives at the MEMORY CONTROL UNIT on connector J25, pin M. The signal goes to card B1, pin 4, where the WRITE POINT mode INDICATOR light is extinguished. The signal also goes to NAND circuit on card B4, pin D, where it is NANDed with the pen ENABLE signal. If both the WRITE POINT and ENABLE signals are present, video gate circuit at card A2, pin U, opens, allowing the shaped pen pulses from card A1 to pass to the Z-AXIS DRIVER circuit on card A5, pin 12, which writes in the POINT MEMORY. The pulses generated by the LIGHT PEN enter the MEMORY CONTROL UNIT at connector J21. From here they pass to video gate on circuit A2, pin 2, which is normally open. From the gate they pass to card A1 where a narrow pulse is generated which appears at card A1, pin 10. This narrow pen pulse triggers multivibrator B2, pin 16, which closes gate A2, pin 2, thus preventing all but the first pen pulse from passing on to the remaining circuitry for a duration of about 200 μs. The narrow pulse also goes to video gate A2, pin 12, where it is used in the point locating circuitry, which will be explained later. Finally the narrow pulse goes to the VIDEO ADDER circuit on card A8, pin 2. Here it is added to the video output allowing the operator to see the pen location on the MONITOR. This aspect of the system will also be explained later. Thus, at the SHAPER circuit on card A1, pin 10, there is, at most, one narrow pen pulse per television field. The output of the SHAPER circuit is a 2 μs pen pulse at pin 17 and a 2 μs HOLD GATE at pin 15. The 2 μs pen pulse (called the wide pen pulse) is used to write in the memories. The HOLD GATE goes to the HORIZONTAL RAMP GENERATOR on card C3, pin 8, where it causes the horizontal deflection signal to pause at its current level for the duration of the HOLD GATE. This allows the writing beams in the memories to remain in one place long enough to accumulate sufficient charge on the storage mesh to cause storage.

Returning to the explanation of the WRITE POINT mode one can see that the wide pen pulse passes through gate A2, pin 16, to the Z-AXIS DRIVER circuit on card A5, pin 12. This circuit gates on the writing beam in the POINT MEMORY for 2 μs, during which time the beam does not move. (A more thorough discussion of the HOLD GATE will be found in the APPENDIX, Sec. A2.11.)

3.2.2.2.2.2 WRITE DISPLAY Mode

Similarly, in the WRITE DISPLAY mode the WRITE DISPLAY signal appears at connector J25, pin L. In this case the gate on card A2, pin 14, allows pulses to pass to the Z-AXIS DRIVER at card A5, pin 14, and thence to the DISPLAY MEMORY.

3.2.2.2.3 CONSTRUCTION Mode

The CONSTRUCT signal generated at the DISPLAY CONSOLE enters the MEMORY CONTROL UNIT at connector J25, pin K. It causes indicator B1, pin 10 to go out and passes to NAND circuits on card B4, pin W, and card B5, pin 17. At B4, pin W, the signal is NANDed with the PROCESSOR WRITE GATE signal. The PROCESSOR WRITE GATE signal is present when the PROCESSOR is ready for a construction and the operator depresses the EXECUTE CONSTRUCTION button on the DISPLAY CONSOLE. If these two conditions are met, video gate A3, pin M, connects the +1.7 volt power supply of card A10 to the Z-AXIS DRIVER on card A5, pin 14, which then gates on the writing beam in the DISPLAY MEMORY. At card B5, pin 17, the signal is NANDed with the EXECUTE CONSTRUCTION READY signal from the PROCESSOR. This signal is present after the PROCESSOR has determined a line or circle. The line or circle may then be written into the DISPLAY memory at the command of the operator. If the CONSTRUCT and EXECUTE CONSTRUCT READY signals are both present, the output of the NAND circuit on card B5, pin 17, causes the DEFLECTION CONTROL RELAY and the DISPLAY GATE CONTROL RELAY to operate as explained in Sections 3.2.2.1.2 and 3.2.2.1.3.

The CONSTRUCT mode signal also goes to the NAND circuit on card B10, pin 4, where it is combined with the pen ENABLE signal. If both the ENABLE signal and the CONSTRUCT signal are present, video gate A2, pin P, will open and allow narrow pen pulses to pass to the VIDEO-TO-LOGIC CONVERTER on card A4, pin 2. The VIDEO-TO-LOGIC CONVERTER converts the narrow pen pulses to narrow logic pulses which are then sent to card B10, pin U. Thus, assuming that ARTRIX is in the CONSTRUCT mode, a series of narrow logic level pulses (a maximum of one per field) will appear at card B10, pin U, when the ENABLE signal is present. Connector J58 supplies video from the POINT MEMORY to the DISCRIMINATOR AND SHAPER circuit on card A15, pin 7, where the video is converted to a series of video level pulses corresponding to white points on the MONITOR. This video is fed to the VIDEO-TO-LOGIC CONVERTER at Card A4, pin 6, where it is changed to logic levels and sent to the NAND circuit on card B10, pin T. The output of this NAND circuit corresponds to the coincidence of a point in the POINT MEMORY and a pulse from the pen. In other words, an output from this NAND circuit appears when the pen "sees" a point in the POINT MEMORY. The output of this NAND circuit (card B10, pin U) goes to the NAND circuit on card B10, pin L. Whether it can pass through card B10, pin L, is determined by card B10, pin M, which is controlled by the R-S flip-flop on card B-10, pins C-J. In the reset state this flip-flop allows pulses to pass through card B10, pin L. However, the first pulse through card B10, pin L, also sets the flip-flop. Thus only one pulse can pass through the gate on card B10, pin L, each time the flip-flop is reset. Releasing the pen ENABLE button resets the flip-flop. The release of the ENABLE button triggers a 2 millisecond ONE SHOT circuit on card B2, pin 11, which resets the gate control flip-flop on card B10, pins C-J. This logic allows but one pulse per operation of the pen ENABLE button. This pulse occurs only when a point in the POINT MEMORY is within the field of view of the pen.

3.2.2.2.4 VIDEO OUTPUT Circuits

The video output of the MEMORY CONTROL UNIT which passes to the DISPLAY CONSOLE is present at connector J22. This video is composed of several video signals. First, the POINT video at connector J59 is combined with the DISPLAY video from connector J61 in the VIDEO ADDER AND SYNCHRONIZATION INSERTER circuit on card A7. No synchronization signal is added at this point. The output of card A7 is combined with the narrow pen pulse in the VIDEO ADDER and SYNCHRONIZATION INSERTER circuit on card A8. Here the synchronization signal from connector J50 is added to the video signal to form the composite video signal supplied to the DISPLAY CONSOLE through connector J22.

3.3 The PROCESSOR

The PROCESSOR of the ARTRIX system consists of two classes of circuits: digital circuits (control circuits, counters, and switching networks) and hybrid digital-analog circuits (D/A converters, the DCVGLA, DCDCAS, COMPARATOR and SINUSOID GENERATOR). As described above, the PROCESSOR may be considered in two sections, the digital section and the hybrid section. The digital section provides digital control signals and digital representations of coordinates, lengths of lines, and radii of circles. The hybrid section uses these digital signals to generate the corresponding analog signals.

The analog signals generated for a circle are:

$$X = R \cos(\omega t) + X_1$$

$$Y = R \sin(\omega t) + Y_1$$

Those for a line are:

$$X = \frac{(X_2 - X_1)}{2} \sin(\omega t) + \frac{X_1 + X_2}{2}$$

$$Y = \frac{(Y_2 - Y_1)}{2} \sin(\omega t) + \frac{Y_1 + Y_2}{2}$$

The means for generating these equations is illustrated in Figure 3.11.

The Appendix contains a list of all logic signals used in the PROCESSOR and a brief explanation of each. Here the internal operation of the PROCESSOR control circuits will be explained in terms of these logic signals. Operations within the PROCESSOR will be described in detail for each mode of ARTRIX.

3.3.1 The Digital Section of the PROCESSOR

3.3.1.1 Synchronizing Signals

When the operator turns the system on, the PROCESSOR begins several continuous operations. These are: providing a digital count corresponding to the horizontal and the vertical position of the electron beam in the DISPLAY, and providing synchronization for the entire ARTRIX system. Synchronizing signals are supplied to the CAMERA CONTROL UNIT. the PROCESSOR contains an 8.064 MHz oscillator, designated TM, which goes through a phase adjusting circuit to form the HORIZONTAL TRIGGER clocking pulse, designated TH. $(TH=(A_{1-8}^{HM}\cdot CS+\overline{A}_{1-8}^{HM})\overline{TM})$. Phase adjustment is necessary because the synchronizing frequence required by the television CAMERA CONTROL UNIT is twice the television line frequency. If the phase were not monitored and corrected automatically, the CAMERA CONTROL UNIT could be synchronized in error by one half a television line. The TH clocking pulses are counted down by the HORIZONTAL MASTER COUNTER (HM) which has 9 bits. The output of its last state corresponds to the television line frequency.

The vertical count corresponding to the vertical deflection of the television system is contained in the VERTICAL MASTER COUNTER (VM). Because of interlacing, there are even and odd fields. Consequently, the VM COUNTER counts by twos and the least significant bit corresponds to an even or odd field. There is one other condition to be satisfied. The VM COUNTER must overflow during vertical blanking (VB) and wait until

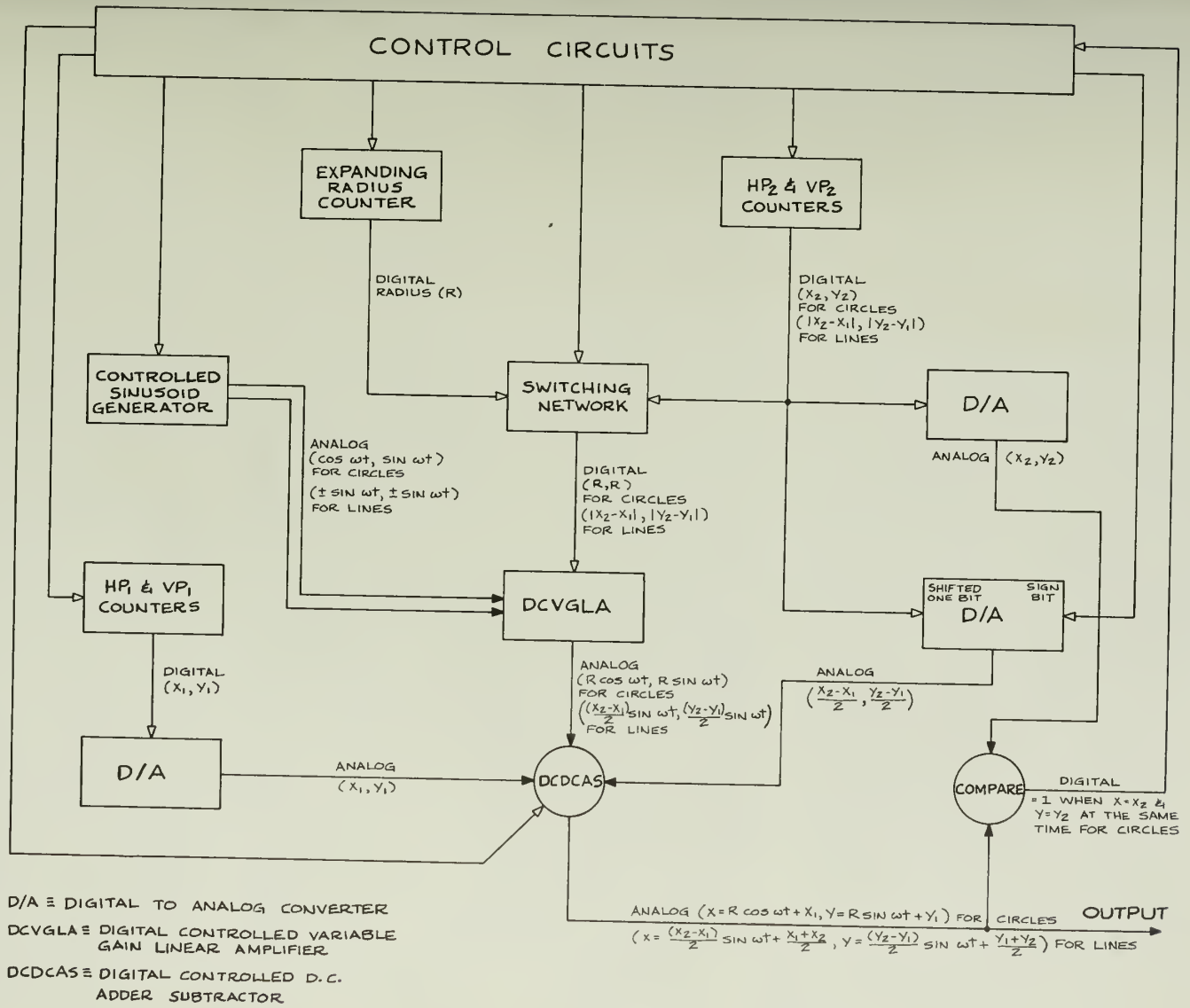


Figure 3.11 The ARTRIX PROCESSOR

the end of the VB before continuing. This is necessary since the VM COUNTER has 9 stages (512 counts, one count per line) whereas there are 525 television lines including VB. Overflow is accomplished by forming the VERTICAL TRIGGER clocking pulse, TV = $\overline{Q}_8$HM($\overline{A}_{1-8}$VM+A) where $\overline{Q}_8$HM is the line frequency, A_{1-8}VM is the VM overflow signal, and A is the output of a flip-flop. This flip-flop is reset by A_{1-6}VM and set by the trailing edge of the VB signal. To get the VM COUNTER to count by twos, the TV clocking pulses are fed to the second stage (from the low order end). To get the least significant stage to correspond to the proper field, the signal E=Q_8HM·Q_7HM and $\overline{E}$ are formed. These signals drive the J and K sides of a J-K flip-flop which is triggered by the VB signal.

Due to delays inherent in the CAMERA CONTROL UNIT, the television synchronization pulse generated therein lags the synchronization pulse from the PROCESSOR. The synchronization signal from the PROCESSOR is generated as Q_6HM·Q_7HM to compensate for these delays.

3.3.1.2 Control Flip-Flops

Depressing the CONSTRUCT button has no direct effect on the PROCESSOR. The operator selects a PROCESSOR mode by depressing the CIRCLE or LINE mode button. These two buttons set opposite sides of an R-S flip-flop whose outputs are CR (for circle) and $\overline{CR}$ (for line). These are two primary logic signals which, in addition to performing control functions, light the CIRCLE or LINE indicator on the PROCESSOR rack.

In either the CIRCLE or LINE mode, when the RESET PROCESSOR button is depressed, the logic signal OP-RP resets five R-S flip-flops. In addition, this signal serves other logical functions, for example, resetting the ER COUNTER. Two of the flip-flops are the overflow flip-flops (OF1 and OF2). The outputs of these flip-flops are used to reset the HP_1, VP_1, HP_2, and VP_2 COUNTERS. These outputs are also used to generate control signals for these counters. OF1 and OF2 are set

by OFHM and VM (i.e. when the HM and VM COUNTERS overflow simultaneously) at the beginning of each frame. The other three flip-flops are used when points are indicated by the operator.

After the PROCESSOR has been reset, the operator may indicate construction points. Points are indicated by directing the LIGHT PEN to a point on the DISPLAY, which is stored in the POINT MEMORY, and pushing the ENABLE button on the LIGHT PEN. One pulse is sent to the PROCESSOR each time the ENABLE button is depressed, thus the LIGHT PEN "sees" a point. In the PROCESSOR the first of the three flip-flops mentioned above is set by the leading edge of the first pulse, the second flip-flop is set by the trailing edge of the first pulse, and the third flip-flop is set by the leading edge of the second pulse. Thus, the first of these flip-flops (P_1) indicates when POINT 1 has been indicated and the third (P_2) indicates when POINT 2 has been indicated. All five flip-flops are always set in the same manner. However, there are other conditions under which they can be reset. The OF1 and P_1 flip-flops are reset by the operator whenever the PROCESSOR or POINT 1 is reset. Flip-flops OF1 and P_2 are reset whenever the PROCESSOR or POINT 2 is reset.

3.3.1.3 Counter Operation

In the following paragraphs the operation of each counter will be explained for the LINE and CIRCLE modes.

The HORIZONTAL POINT 1 COUNTER (HP_1) contains a binary number corresponding to the horizontal position of POINT 1. When the operator resets either POINT 1 or the PROCESSOR, $\overline{OF_1}$ becomes a logical "one" until the beginning of a frame. This signal is used to reset HP_1. HP_1 counts the signal TH; $\xi H = \overline{P}_1 \cdot OF_1$ is the control signal. Thus, HP_1 starts counting from zero (having been reset) at the beginning of a frame and stops when P_1 is indicated.

The VERTICAL POINT 1 COUNTER (VP_1) contains a binary number corresponding to the vertical position of Point 1. VP_1 counts signal TV

and is controlled by $\xi V=\xi H\cdot(\overline{\overline{OF}}) + \overline{A}_{\overline{1}-\overline{8}}VP_1$. When OF_1 is a logical "zero", VP_1 will count until the output of its eight most significant stages are all zero. At the beginning of the next frame, it counts until POINT 1 has been indicated. The $(\overline{\overline{OF}_1})$ signal insures that VP_1 has been completely reset before it begins counting. The least significant bit is clocked by the VB signal and controlled by a signal E which indicates the even and odd fields of a frame.

The HORIZONTAL POINT 2 COUNTER (HP_2) contains a binary number which corresponds to the horizontal position of POINT 2 in the CIRCLE mode. In the LINE mode, the binary number corresponds to the magnitude of the difference in the horizontal positions of POINT 2 and POINT 1. Similarly, HP_2 is reset by $\overline{OF}_2$, counts TH, and is controlled by $\eta H=OF_2\cdot\overline{P}_2(CR+P_1)$. When POINT 2 or the PROCESSOR is reset in the CIRCLE mode, HP_2 is reset and starts counting at the beginning of a frame and stops counting when POINT 2 is indicated. When POINT 1 and POINT 2 or the PROCESSOR are reset in the LINE mode, HP_2 is reset and starts counting when POINT 1 is indicated and stops counting when POINT 2 is indicated. If P_2 is reset and P_1 is not, HP_2 starts counting at the beginning of a frame. Note that if the horizontal deflection of POINT 1 is larger than that of POINT 2, HP_2 is the complement of the difference in deflections.

The VERTICAL POINT 2 COUNTER(VP_2) contains a binary number corresponding to the vertical position of POINT 2 in the CIRCLE mode. In the LINE mode, this number corresponds to the magnitude of the difference between vertical deflections of POINT 1 and POINT 2. Similarly, VP_2 counts signal TV and is controlled by $\eta V=\eta H\cdot(\overline{\overline{OF}_2}) + \overline{A}_{\overline{1}-\overline{8}}VP_2$. Thus when OF_2 becomes a logical "zero", VP_2 counts until the outputs of its eight most significant stages are all zero. It then stops counting until the beginning of the next frame when it starts counting according to ηH. The $(\overline{\overline{OF}_2})$ term insures that VP_2 starts counting only after it has been reset to zero (i.e. completely reset). Since the VP_2 control signal contains a term ηH, it counts as explained above for HP_2. Like VP_1, the

least significant stage of VP_2 is clocked by the VB signal and is controlled by $\Phi = CR\,\overline{E} + \overline{CR}\,P_1$ and $O = CR \cdot E + \overline{CR} \cdot P_1$ for even and odd frames respectively. In the CIRCLE mode, VP_2 operates like VP_1. In the LINE mode, POINT 1 and POINT 2 are separated by an even number of lines for an even number of fields and an odd number of lines for an odd number of fields, independent of the field (even or odd) in which POINT 1 was indicated.

The ER COUNTER contains a binary number corresponding to the radius of the circle to be constructed. It counts signal EF and is controlled by $CR \cdot P_2 \cdot \overline{RS}$. RS is the output of an R-S flip-flop which is reset by PROCESSOR RESET or RADIUS RESET button and is set by $H_{coinc} \cdot V_{coinc} \cdot P_1 \cdot P_2$ (i.e., when a circle of expanding radius centered at POINT 1 goes through POINT 2). The ER COUNTER will begin counting again when the RADIUS RESET button is depressed.

3.3.1.4 Slope Control Circuits

Other PROCESSOR control circuits determine the sign of the difference between the deflections of POINT 1 and POINT 2 in the LINE mode of operation. In the horizontal case, for example, it is necessary to determine whether HP_2-HP_1 is positive or negative. An R-S flip-flop is reset by $A_{1\text{-}8}HP_2$ (i.e., HP_2 is reset, implying that the horizontal deflection of the system corresponds to the contents of HP_1) and set by $A_{1\text{-}8}HM \cdot P_2$ (i.e., when HM is set to zero, implying zero horizontal deflection). Thus the output of the flip-flop is a logical "zero" when HP_2-HP_1 is positive and is a logical "one" when HP_2-HP_1 is negative. The output of the flip-flop is ANDed with $\overline{CR}$ to ensure that it is a "one" only in the LINE mode. The results are CH and $\underline{CH}$.

Similarly, in the vertical case, it is necessary to determine whether VP_2-VP_1 is positive or negative. This is accomplished in the same manner as for the horizontal case. An R-S flip-flop is reset by

$\overline{(A_{\bar{1}\text{-}\bar{8}}VP_2)\cdot MMr}$. MMr is the output of a monostable multivibrator which is triggered by the one to zero transition of $\bar{Q}_8$ HM. The output duration is apprximately 125 nanoseconds. This is necessary to eliminate erroneous pulses in $A_{\bar{1}\text{-}\bar{8}}VP_2$ which arise because VP_2 is a ripple counter. The R-S flip-flop is reset when the outputs of VP_2 are all zero (except for the least significant bit) and the vertical deflection corresponds to the contents of VP_1. The flip-flop is set by $\overline{(A_{\bar{1}\text{-}\bar{8}}\ VM)(MMV)(P_2)}$, that is, when VM is set to zero, implying no vertical deflection. Thus the output of the flip-flop is a logical "zero" when HP_2-HP_1 is positive and is a logical "one" when HP_2-HP_1 is negative. The output of the flip-flop is ANDed with $\overline{CR}$ to ensure that it is a "one" only in the LINE mode. The results are CV and $\underline{CV}$.

3.3.1.5 Miscellaneous Circuits

The signal CHG = $A_{0\text{-}3}HM + A_{0\text{-}3}VM$ may be used to present a grid raster on the MONITOR.

The switching network of the PROCESSOR provides the signals for the DCVGLA. The i^{th} input to the HORIZONTAL DCVGLA is given by $H_i=\underline{CH}\cdot\bar{Q}_i\cdot HP_2 + CH\cdot Q_i\cdot HP_2 + CR\cdot\bar{Q}_i\cdot\overline{ER}$. The i^{th} input to the VERTICAL DCVGLA is given by $V_i=\underline{CV}\cdot\bar{Q}_i\cdot VP_2 + CV\cdot Q_i\cdot VP_2 + CR\cdot\bar{Q}_i\cdot ER$.

The digital signals for the D/A converters are taken directly from the appropriate counters.

The remaining circuits in the PROCESSOR deal with the interaction between the PROCESSOR and other parts of the system. When the EXECUTE CONSTRUCT button is depressed by the operator, the construction being generated is written into the MEMORY by the PROCESSOR WRITE GATE signal (PWG). This happens only when the PROCESSOR is ready to execute the construction. The EXECUTE READY signal is given by $XR=CR\cdot P_1\cdot RS + \overline{CR}\cdot P_1\cdot P_2$. The PWG signal is the output of an R-S flip-flop which is set by $\overline{(OP\text{-}XC)\cdot XR}$ and reset by $\overline{(OP\text{-}\overline{XC})}$. Using an R-S flip-flop eliminates the contact bounce of the manual push button switch.

The PR signal indicates when the PROCESSOR has been reset and is given by $PR = \overline{P}_1 \cdot \overline{P}_2 \cdot \overline{R}_s$

3.3.2 Hybrid Section of the Processor

The hybrid section of the PROCESSOR is shown in Figure 3.12. All control inputs are from the digital section of the PROCESSOR and are in the digital form. All outputs (except those from the comparators) are analog, and go to the DISPLAY MEMORY via the DEFLECTION CONTROL RELAY in the MEMORY CONTROL UNIT. Solid arrows represent analog signals and open arrows represent digital signals. In the following discussion, ARTRIX is assumed to be in the CONSTRUCT mode of operation.

3.3.2.1 Circle Operation

When the PROCESSOR is in the CIRCLE mode, sine and cosine waveforms are selected by means of relays and the logic signals CR, CV, and CH. Figure 3.13 shows the combination of these signals to form a circle in the MEMORY. The cosine wave is applied to the vertical channel and the sinewave is applied to the horizontal channel. Waveform manipulations are performed in each channel using horizontal and vertical digital inputs. The gain of the vertical channel is only 3/4 that of the horizontal channel. This preserves the 3:4 aspect ratio of the television MONITOR.

The analog signals necessary for circle generation are:

$$X = R \sin(wt) + X_1$$
$$Y = R \cos(wt) + Y_1$$

X_1 and Y_1 are voltages corresponding to the position of the center of the circle. The digital signals HP_1 and VP_1 corresponding to these voltages are generated as described in section 3.3.1.3. HP_1 and VP_1 are now applied to the number 2 HORIZONTAL and VERTIAL D/A CONVERTERS. The output of these D/A converters are two DC voltages corresponding to HP_1 and VP_1. The radius of the circle is determined by coincidence. The sine and cosine voltages are applied to an amplifier

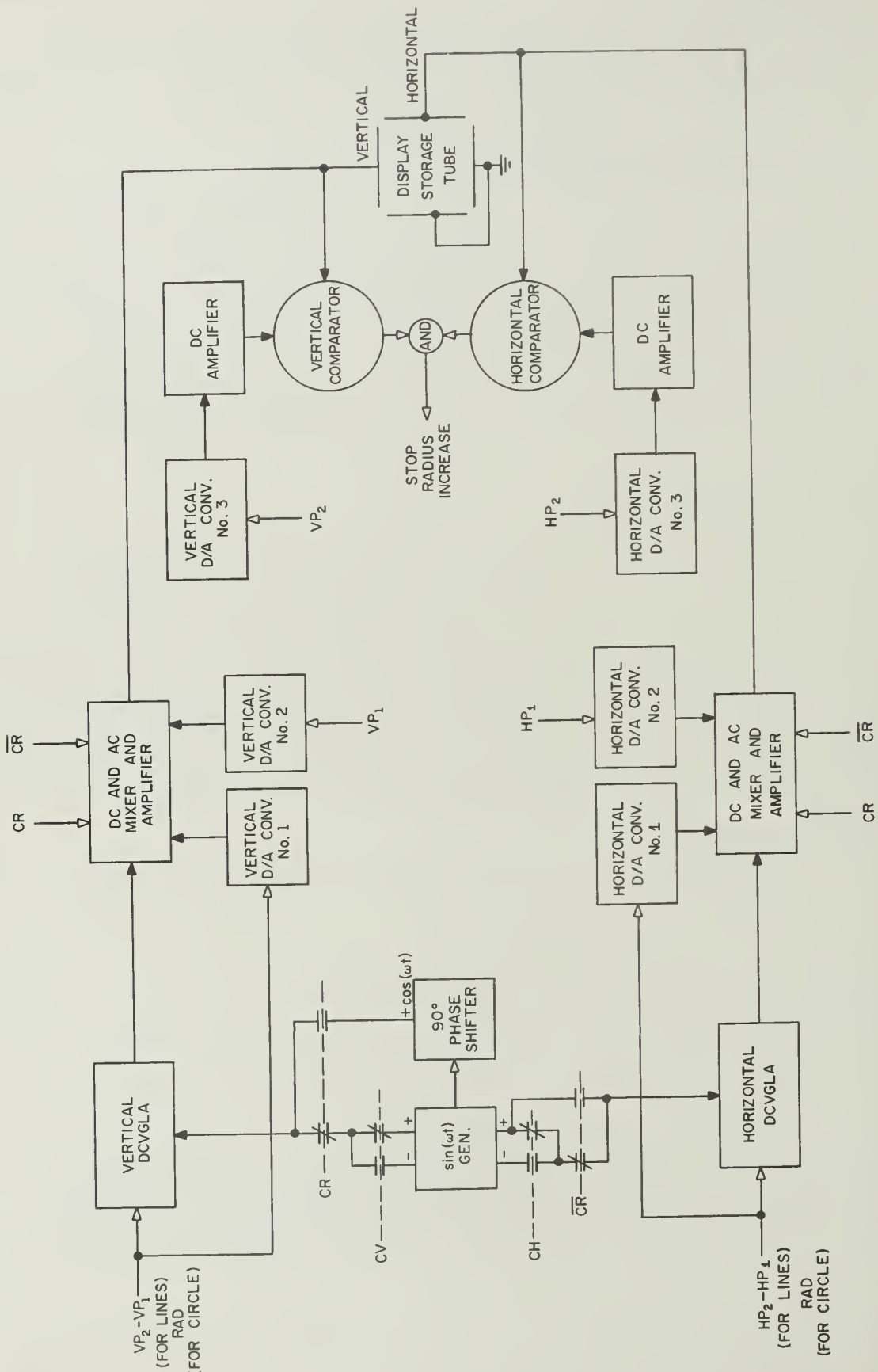


Figure 3.12 Hybrid PROCESSOR

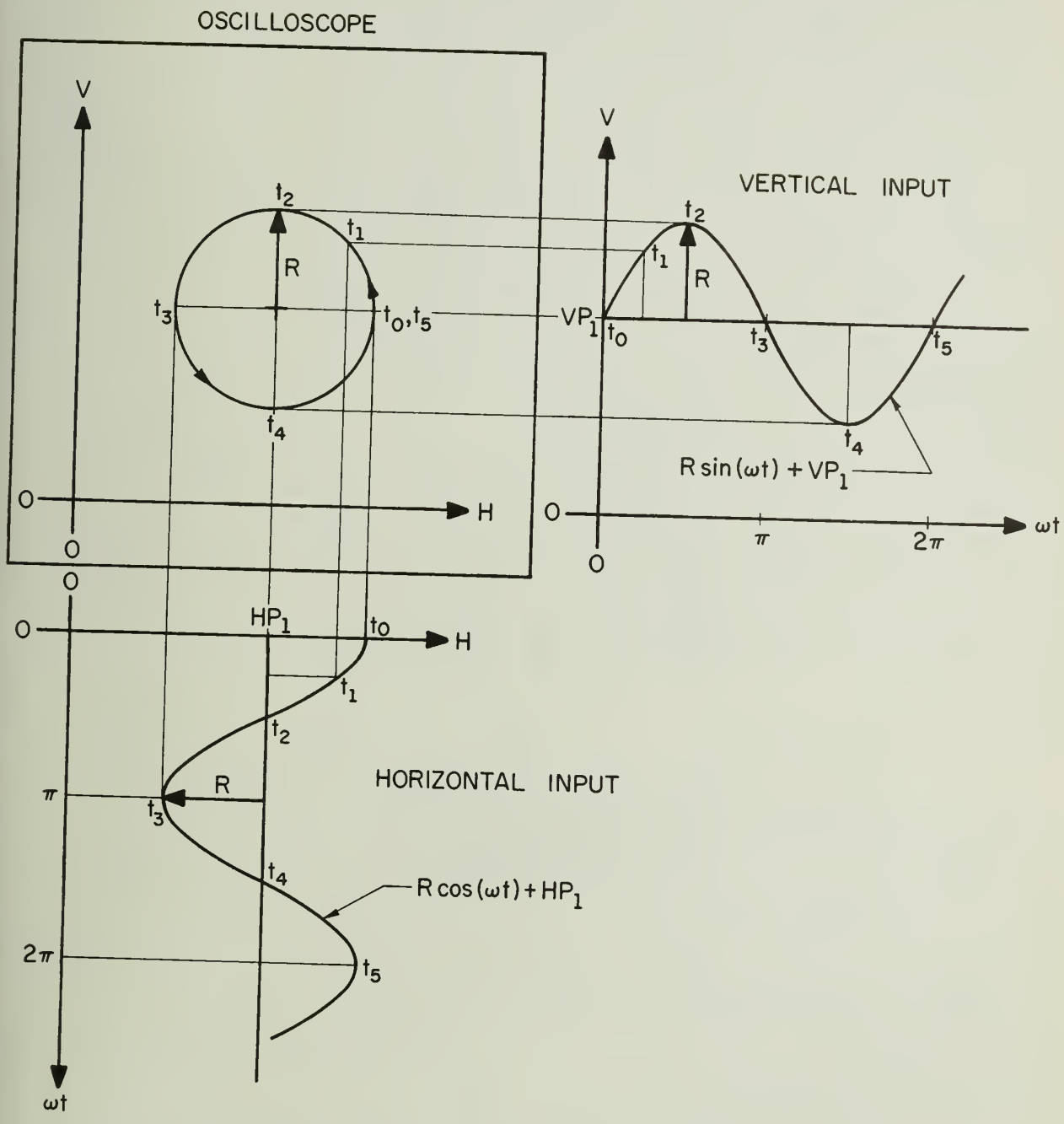


Figure 3.13 Generation of a Circle with Sine and Cosine Functions

whose gain is proportional to a given digital input. This is the Digitally Controlled Variable Gain Linear Amplifier, designated as DCVGLA. The digital inputs to the horizontal and vertical DCVGLAs are identical and are stepped from 0 to 511 when the center of the circle and POINT 2 have been indicated. The outputs of the DCVGLAs are then sinusoids whose amplitudes increase with time. These outputs are mixed in the DC and AC MIXER and AMPLIFIER with signals X_1 and X_2 in the horizontal and vertical channels, respectively. The number 1 VERTICAL and HORIZONTAL D/A CONVERTERS are disabled by CR and $\overline{CR}$ in the circle mode. The output of the MIXER is a sinusoid, whose amplitude increases, with a DC offset. The indicated point on the circumference of the circle is similarly converted by a D/A converter (#3) to a DC level corresponding to the coordinates of that point. These two DC levels are then compared with the sinsoids whose amplitudes are increasing. The desired radius is reached when the amplitudes of both sinusoids equal the DC levels (or coordinates of POINT 2) simultaneously. When this coincidence occurs, a logic signal causes the RADIUS COUNTER to stop. In other words, the circle expands about its center until the indicated size (designated by the HP_2 and VP_2) has been reached.

3.3.2.2 Line Operation

As in the CIRCLE mode, logic signals CR, CV and CH select sine or minus sine functions for line generation. (Actually, the selection of sine or minus sine, depending on the slope of the line, is not determined until POINT 2 is indicated). Figure 3.14 shows the combination of these signals to form a line. The CR and $\overline{CR}$ signals enable both the #1 and #2 D/A CONVERTERS whose outputs go to the DC and AC MIXER and AMPLIFIER. When POINT 1 is indicated, signals VP_1 and HP_1 are available and are applied to the D/A CONVERTERS. The outputs of the D/A CONVERTERS are fed to the MIXER. The output of the MIXER then corresponds to the coordinates of the first endpoint of the line (POINT 1).

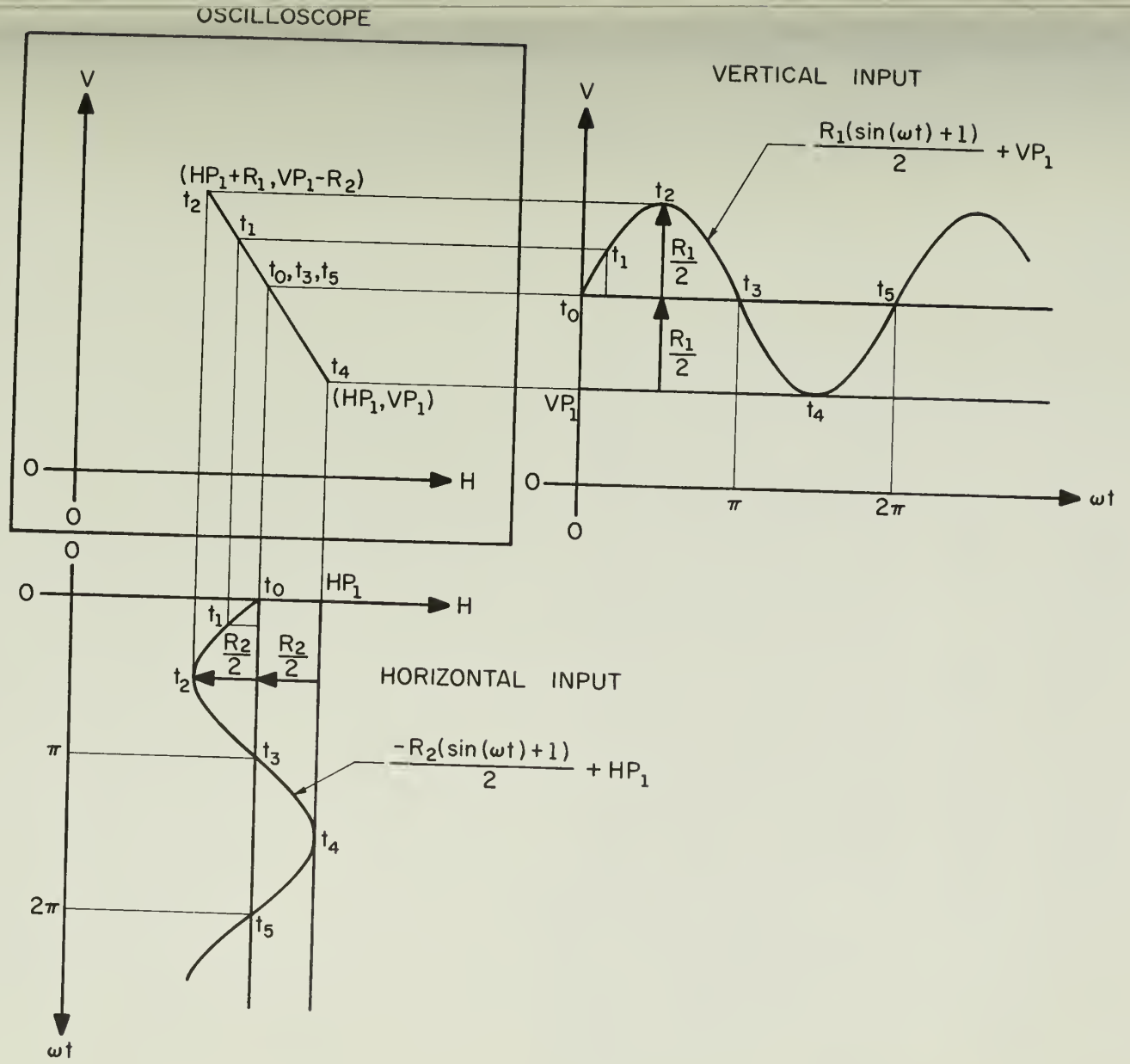


Figure 3.14 Generation of a Line with a POSITIVE and NEGATIVE Sine Function

Recall the equations of a line from section 3.3.0:

$$X = \frac{(X_2-X_1)}{2} \sin(\omega t) + \frac{X_1+X_2}{2}$$

$$Y = \frac{(Y_2-Y_1)}{2} \sin(\omega t) + \frac{Y_1+Y_2}{2}$$

It is evident that POINT 2 must now be indicated to give the digital signals (HP_2-HP_1) and (VP_2-VP_1). These signals are applied to the DCVGLA to give the proper sinewave amplitude, and to the #1 D/A CONVERTERS to give the proper DC offset. This keeps the line from extending through POINT 1. All three output signals are then of the form required for line generation, and are applied to the deflection plates of the DISPLAY MEMORY. No use is made of HP_2 and VP_2 D/A CONVERTERS in the LINE mode, and comparison methods are not required.

4.0 Conclusions

4.1 Summary

The fundamental objective of the ARTRIX project was to prove the feasibility of a self-contained hybrid graphical processing system. The project was carried out on a relatively low cost scale since a separate digital computer was not required for information processing.

One of the difficulties encountered with ARTRIX was that of resolution. The upper limit on the resolution of ARTRIX was poorer than had been anticipated. The minimum achievable line width was 3 television lines for free hand drawings, and 2 television lines for constructions. The principal factor limiting the system resolution was the Memotron storage tube in the Memotron-Vidicon memory device. Under optimum conditions, the best posible resolution of the Memotron storage tube is 50 lines per inch, which when displayed on a television screen having a 3:4 aspect ratio, corresponds to about 280 total television lines. Under actual operating conditions however, this figure was more realistically about 200 lines. Had another method of storage been used, the resolution might have approached that of digital systems. It is significant, however, that in spite of the poor resolution, the cost and bulk of a core memory and its associated input and output equipment, or the cost and bulk of other means of storage for that matter, would far exceed that of the Memotron-Vidicon storage technique. The Memotron and its required circuitry were readily available as a packaged unit, the MEMO-CORDER, and in combination with the Vidicon camera unit, provided obvious advantages as a small, self-contained, ready-built storage unit.

The most frustrating, though by no means insurmountable problem was misregistration of points, drawings and constructions due to drift in DC levels within the system. It was found that this drift problem was minimal when sufficient warm up time was allowed.

The time required however, was about 1.5 hours. The most probable sources of drift error within the system were the camera control units and the DC hybrid circuits. Improved temperature stabilization of the camera circuitry would probaly improve the system performance considerably.

The hybrid approach to the design of ARTRIX was highly successful. Aside from occasional misregistration, the CIRCLE and LINE modes of ARTRIX functioned admirably. The method of digitizing the television raster into X and Y coordinates and digitally controlling analog signal generators to produce lines and circles resulted in far more accuracy than the corresponding system resolution. The entire PROCESSOR was based on 500 television line resolution when, as stated above, the maximum system resolution was 280 lines. The most significant advantages of the hybrid design over an all-digital design are low cost and relatively few components. Clearly, circle and line generation using Lissajous patterns is a trivial exercise compared to circle and line generation by digital means. Higher order curves would, of course, require more complex Lissajous patterns.

The control of video information between the memories and the DISPLAY, and the processing of the LIGHT PEN pulses presented no major problems, contrary to original anticipations. Delays between the video signals were insignificant and required no compensation. Writing points in the memories within the capabilities of the Memotron tubes was accomplished using the beam-hold technique described in section 3.2.2.2.2.1.

The ERASE mode of operation functioned somewhat less than satisfactorily for reasons not clearly understood at this time. It was throught that much information was being lost during the transfer process since the beam-holding technique could not be employed in transferring information between Memo-Corders during the erase cycle. It was found, however, that this was not the significant problem. It

has been determined that information is transferred to the TEMPORARY MEMORY successfully, but fails to be rewritten into POINT or DISPLAY MEMORY.

In spite of the most degrading aspect of ARTRIX, that of resolution, the ARTRIX project was generally very successful. In its final form, ARTRIX produced lines, circles and on some occasions erasures, with precision and regularity surpassing the expectations of its designers.

4.2 Recommendations

An interesting project would be the design of an all-analog system using capacitive storage techniques in place of binary counters to store coordinates of lines and points. With high input impedance devices such as operational amplifiers and field effect transistors, it is felt sufficiently long storage times, with readout, would easily be obtained. In such a system, the linear ramp deflection voltages might serve as coordinate references.

In contrast, an all digital system, while easily constructed due to the high degree of development in digital design, provides unnecessary accuracy at a premium cost. As in digital systems, the greatest need in ARTRIX is an improved storage medium for pictorial information.

Several semi-analog devices which might be considered as alternatives to the Memotron-Vidicon combination are the scan-converter tube, the tape recorder or the disc recorder.

Although the scan-converter is unsurpassed with respect to resolution, its usefulness is limited by its relatively short storage time. Typical storage times are from three to five minutes. Furthermore, poor registration between the read and write modes is a limiting factor for accurate local erasure.

A video tape recorder with sufficiently high resolution would be an alternative were it not for its lack of any selective erase capability. Its storage time is, of course, virtually unlimited.

The video disc recorder is the most promising alternative, providing its resolution is sufficiently high. Multi-track disc recorders are available with selective erase facilities. The multi-track feature would be extremely advantageous in a system such as ARTRIX, where more than one memory unit is required. Also additional tracks can be added to the disc recorder at a nominal cost.

APPENDIX

A1.0 Power Distribution System

A1.1 AC Power Distribution

Figure A1.1 shows the AC PANEL and the AC ON-OFF PANEL. All AC power supplied to ARTRIX is controlled by the relay located in the AC PANEL. This relay will operate if the AC ON-OFF switch is in the ON position and the VOLTAGE MONITOR (located in the MAIN JUNCTION BOX) senses no irregularities in the DC supply voltages. (For turn-on the VOLTAGE MONITOR is bypassed. See Section A1.3). If these two conditions are met, the relay in the AC PANEL energizes. This applies AC power to the three AC strips in the MAIN CONSOLE and to the AC strip in the DISPLAY CONSOLE (see Figure A1.2). The transformer in the AC PANEL supplies the AC ON-OFF indicator light with power. The ON-OFF indicator is controlled by the ON-OFF switch.

The VOLTAGE MONITOR (see Section A1.3), in addition to monitoring the D.C. power supplies, also monitors the supplies in the CAMERA CONTROL UNITS and the MEMO-CORDERS. The sensing lines for this operation are on connector P80 as shown in Figure A1.1.

A1.2 DC Power Distribution

The DC power supplies all operate when the AC power is applied. The outputs of the supplies go to the MAIN JUNCTION BOX (Figure A1.3), where the voltages are distributed to the MEMORY CONTROL UNIT, the PROCESSOR and the DISPLAY CONSOLE. These voltages are monitored at the MAIN JUNCTION BOX.

The DC power is distributed in the DISPLAY CONSOLE by the DISPLAY CONSOLE JUNCTION BOX (Figure A1.4). The ARTRIX system uses six DC power supplies to supply the following voltages: -5, $\pm$10, -15 and $\pm$25 volts.

A1.3 The VOLTAGE MONITOR

The ARTRIX VOLTAGE MONITOR was designed to provide the system with a self-contained safety device for the protection of the

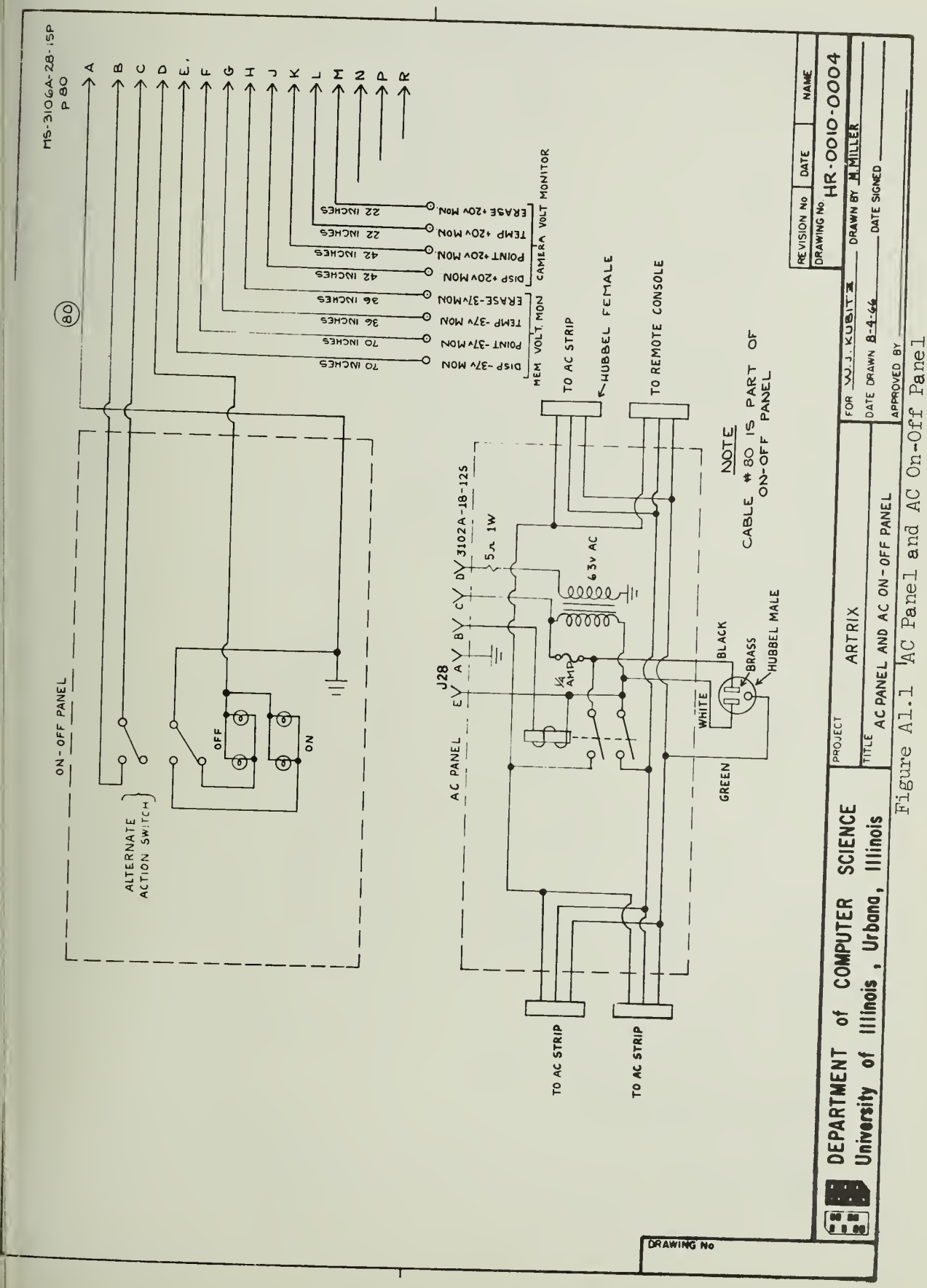


Figure A1.1 AC Panel and AC On-Off Panel

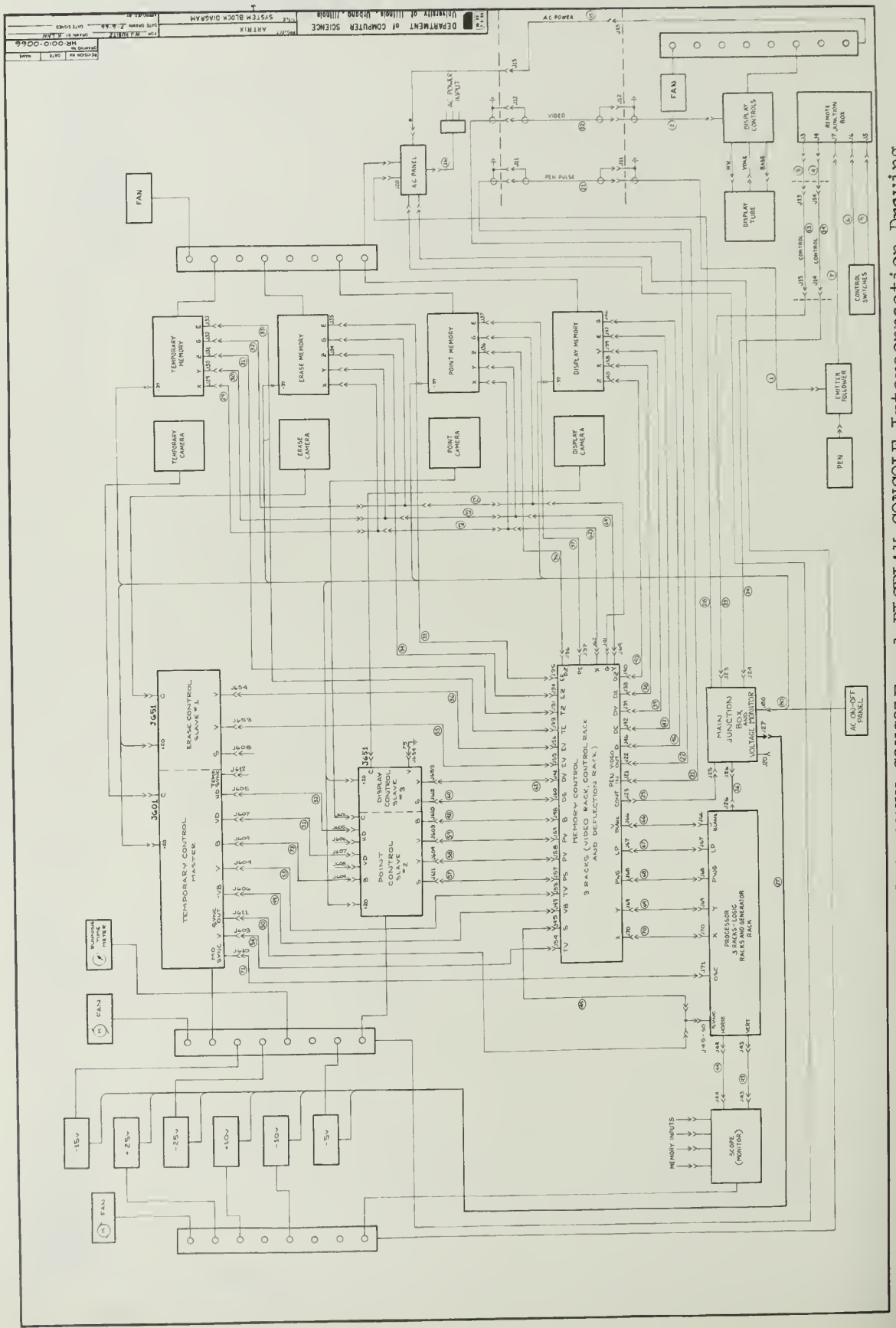


Figure A1.2 MAIN CONSOLE and DISPLAY CONSOLE Interconnection Drawing

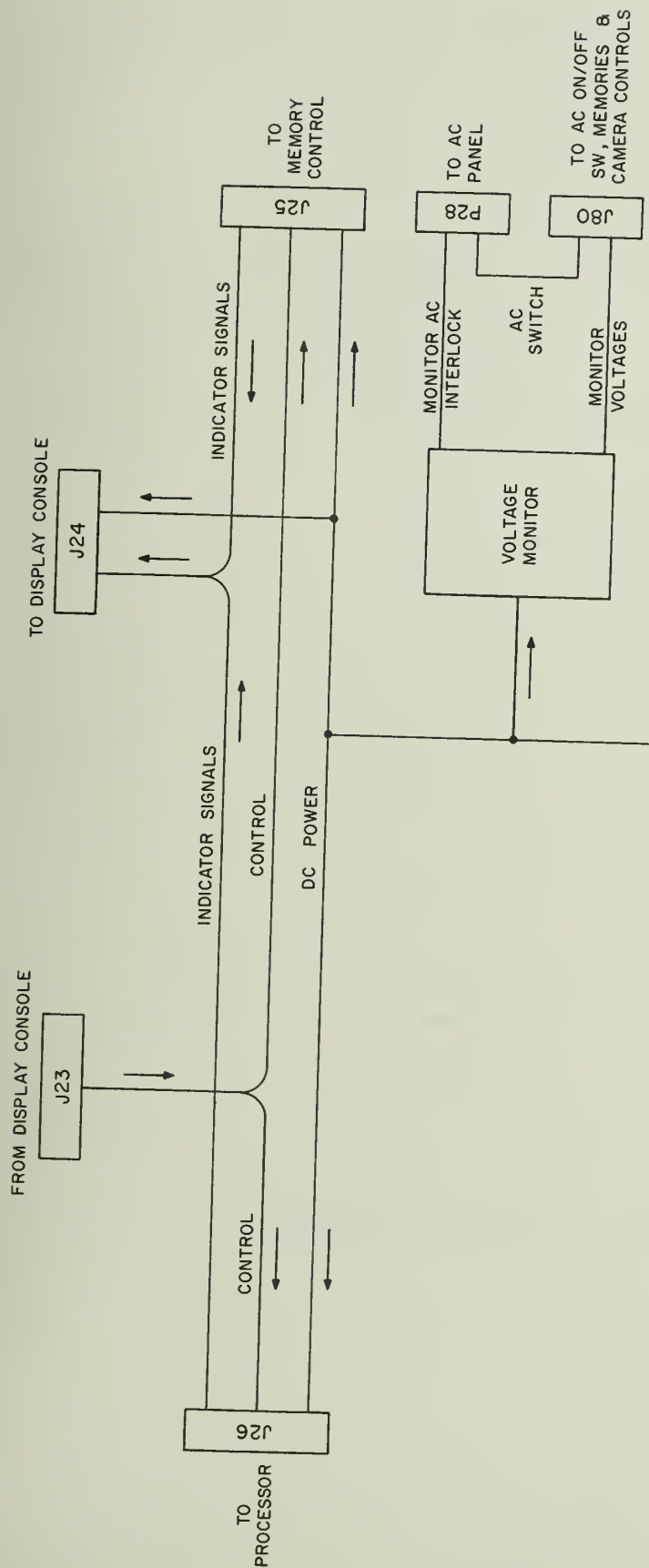


Figure A1.3 Simplified Diagram of MAIN JUNCTION BOX

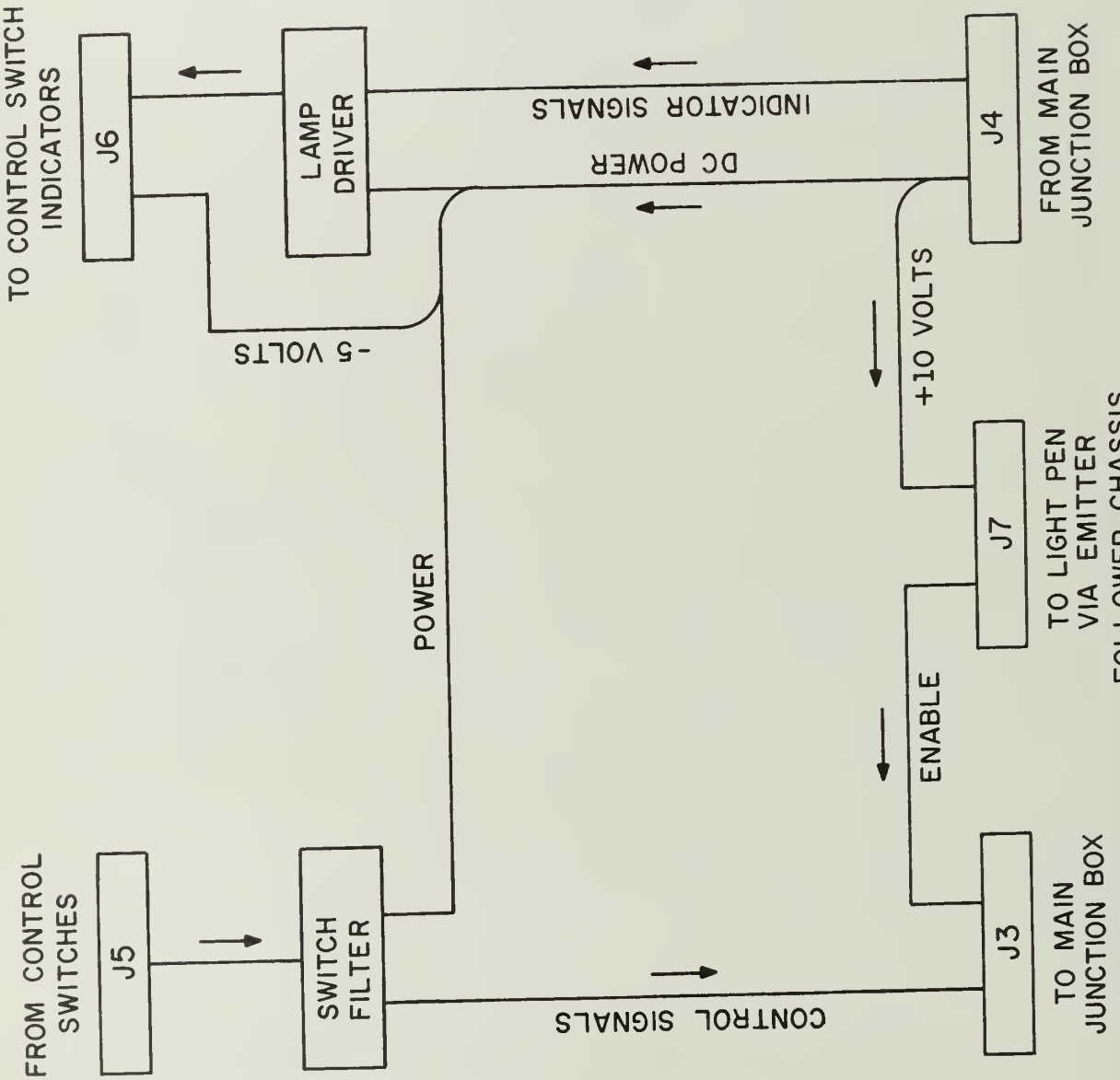


Figure A1.4 Simplified Diagram of DISPLAY CONSOLE JUNCTION BOX

equipment within the system. Although it does not have a 100 per cent fault detection capability, it does give a high degree of protection to the more critical sections of the system, such as the storage tubes, cameras and the circuitry of the PROCESSOR and MEMORY CONTROL UNIT.

The VOLTAGE MONITOR circuit (Figures A1.5 and A1.6) consists of three basic sections: a VOLTAGE SUMMING CIRCUIT, a DIFFERENTIAL AMPLIFIER, and a LOCK-OUT RELAY. Some additional features will be described below.

The SUMMING CIRCUIT is a resistive adder containing a precision resistor for each sense line connected to the VOLTAGE MONITOR. The sense lines are attached to the selected monitor points, such as the logic power supplies, camera power supplies and MEMO-CORDER power supplies. The resistors are selected to provide a 1 milliampere load for each monitored voltage (for example, monitoring 50 volts requires a 50 k resistor, 25 k resistor, etc.). These resistors are connected to a common point. When all the input voltages are present and adjusted, the currents at the common point sum to produce about 0 volts. The change of, or the lack of any of the sensed voltages will cause a change in the voltage level at the common point.

The common point of the SUMMING CIRCUIT provides one of the two inputs to a DIFFERENTIAL AMPLIFIER. The other input is an adjustable DC voltage. After the system is turned on and adjusted, this DC voltage is adjusted to the same voltage level as that of the common point of the SUMMING CIRCUIT. This will balance the DIFFERENTIAL AMPLIFIER, resulting in zero ouput. The output of the DIFFERENTIAL AMPLIFIER drives a relay. The relay is connected such that it latches on its own contacts once closed, hence the term "lock-out".

Any detected change of the sensed voltage levels will energize the LOCK-OUT RELAY. One set of contacts on the LOCK-OUT RELAY is in series with the AC ON-OFF SWITCH. Therefore, any detected change in the monitored voltage will shut down the system.

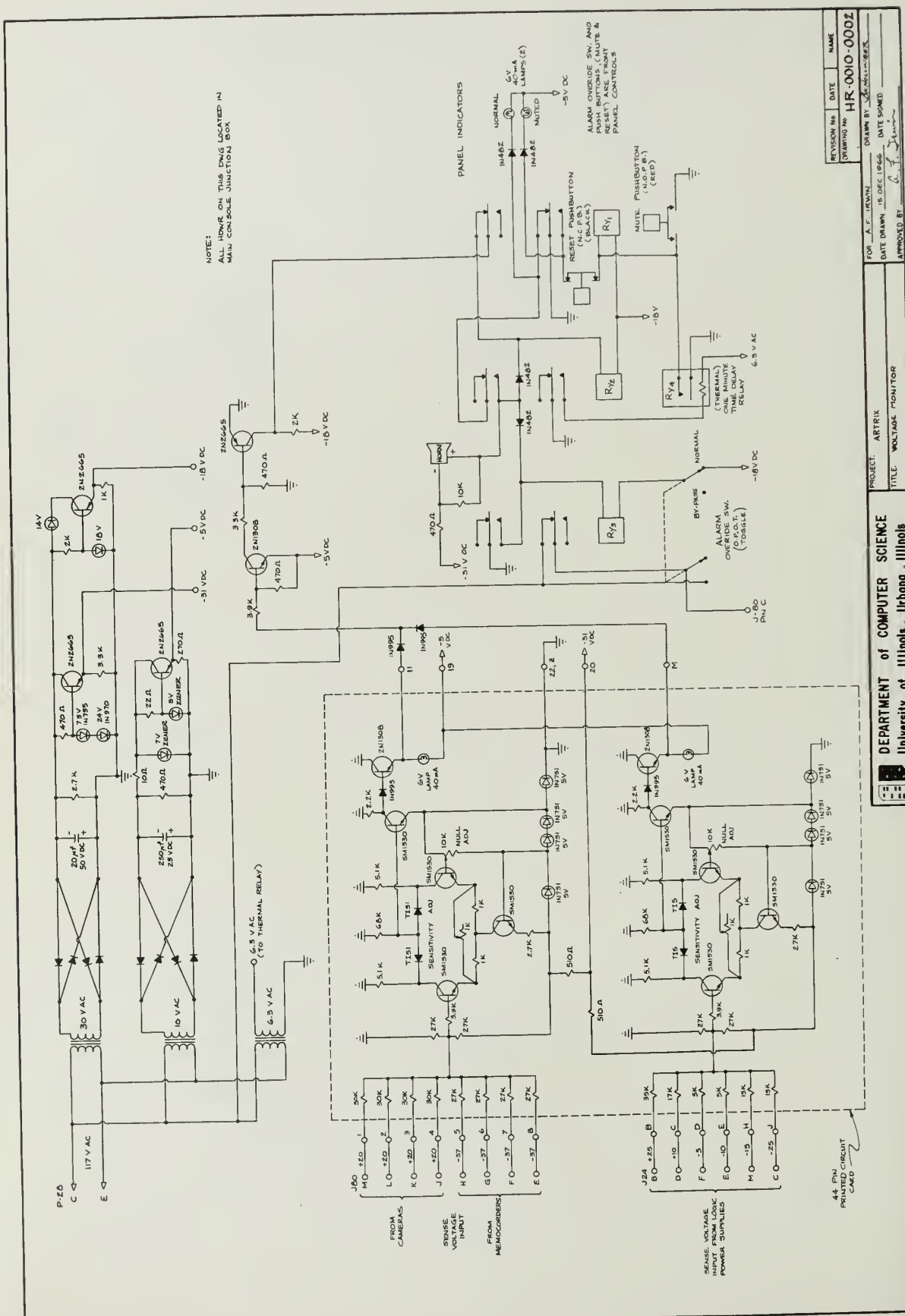


Figure A1.5 VOLTAGE MONITOR Chassis

An alarm horn is connected to the VOLTAGE MONITOR such that a detected malfunction will provide an audible tone, alerting the operator. A MUTE button is provided to silence the alarm once the operator has become aware of a malfunction. A MUTE INDICATOR warns of the muted condition. Since protection is not provided in the muted condition, the VOLTAGE MONITOR must be reset after the malfunction is corrected. The system was found to be more stable if it operates continuously and is not shut down overnight (see Section A4.1). It is conceivable that a fault could occur while the system is unattended. A 60-second time delay relay was installed which mutes the horn after the elapsed time. Should a lock-out condition occur while the system is unattended, the possibility of the horn sounding for hours at a time is thus eliminated.

The VOLTAGE MONITOR has a self-contained power supply which is not disabled by an automatic shut down of the rest of the system. It should be noted that a manual shut down appears as a fault to the VOLTAGE MONITOR, causing a lock-out condition. It is necessary, therefore, to have a VOLTAGE MONITOR BYPASS SWITCH on the VOLTAGE MONITOR panel. This switch must be set in the BYPASS position in order to power up the system. The switch may then be returned to the NORMAL position.

A2.0 Description of Circuits

A2.1 DIAMOND GATE, 1469-14A

The DIAMOND GATE circuit is an analog gating circuit which uses a conventional diode bridge configuration. It differs from conventional analog gates, however, in that the bridge is biased on by a current source and sink. Turning off the DIAMOND GATE is accomplished by shunting the bias current around the bridge.

This circuit is topologically the same as the diamond gate employed in the PARAMATRIX system. For more details see "Hybrid Circuits for the Paramatrix System" by Edward F. Prozeller, Report No. 188, Department of Computer Science, University of Illinois, Urbana, Illinois, September 7, 1965.

A2.2 DCVGLA (Digitally Controlled Variable Gain Linear Amplifier)1469-102

The DCVGLA controls the amplitude of a sinewave by means of a digital input. There are 512 increments corresponding to 9 digital bits. A mathematical transfer function for this device would be as follows:

$$X = K\sin(\omega t)\left[A_0 2^0 + A_1 2^1 + A_2 2^2 + \ldots + A_8 2^8\right]$$

where $a_0 \ldots\ldots a_8$ are the binary inputs, K is an arbitrary gain constant and X is the output.

The output has a peak to peak variation from zero to $\pm$ 10 volts. A gain constant of $K \approx 1.5$ is used which requires a 6.67 volt peak input sinewave.

Currents are summed through resistors to obtain the above function. The resistor values are in the ratio of $2^0 : 2^1 : 2^2 : \ldots : 2^8$. Transistors switch these resistors in and out of the circuit. The scheme is similar to that in a D/A converter, except that an AC voltage is converted instead of a DC voltage. The digital control of the

voltage is independent of the phase and amplitude of the AC voltage. A basic diagram of the scheme used is shown in Figure A2.1 and the actual circuit used is shown in Figure A2.2. The constant controlled voltage source in the circuit is an emitter follower whose emitter resistances are the digitally selected resistors. A Darlington configuration of the transistors was chosen to make the impedence of the source as low as possible. This gives the circuit a curren gain of about $\beta_1 \cdot \beta_2$ where β_1 and β_2 are the respective betas of the 2N2102 and 2N3054 transistors. This proved to be adequate for variations in the emitter resistance from $R_0/2$ to open circuit. A DC bias current is used to keep the transistors in the active region. The 8 Hy coil in series with the bias resistor appears as an AC open circuit at 10 KHz.

Current is sensed at the collector of the Darlington pair. A transformer is the current detection device. It provides complete DC isolation from the rest of the circuit, gives large voltage gain, and provides the required impedence match. The AC resistance in the collector is small compared with the minimum AC resistance in the emitter. The load on the secondary of the transformer is 10K ohms. The turns ratio of the transformer is such as to present 3 ohms in the primary; 3 ohms in the collector is small compared with a minimum of 100 ohms in the emitter. Using this value as a reference, the R_0 in the digital emitter chain was chosen close to 200 ohms. Since it is difficult to procure precision resistors such that R_0 is 200 ohms $\pm$ 0.1%, and since the saturation resistance of the transistor switch would add an even greater error, it was decided to use adjustable resistors in the first six most significant bits of the chain. For the last three bits 1% resistors were found adequate, and at this value ($2^6 R_0$) the saturation resistance of the transistors is also negligible. The resistance chain is adjusted such that any two adjacent bits provide an output voltage in the ratio of 2:1. The switching in

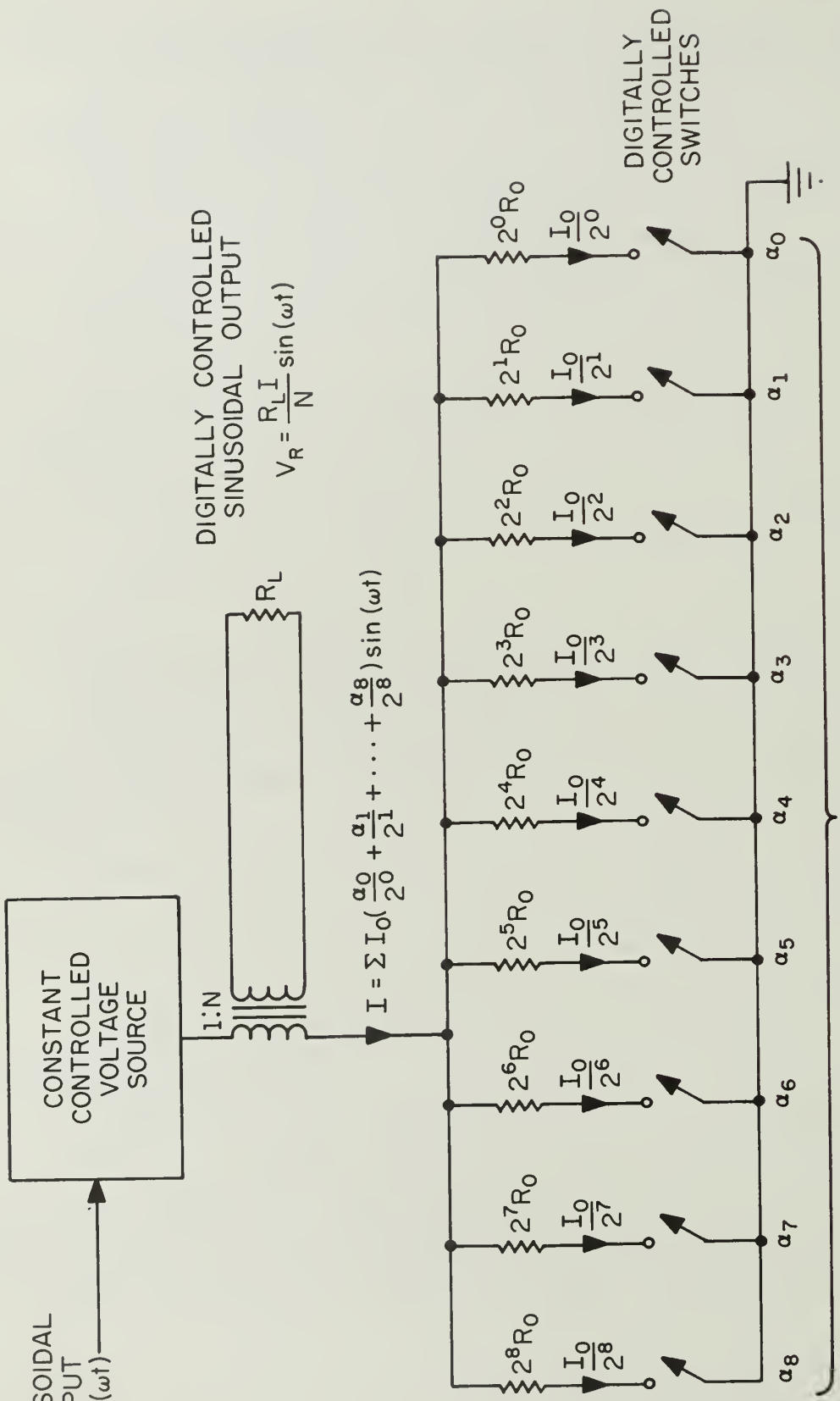


Figure A2.1 Basic Scheme of DCVGLA

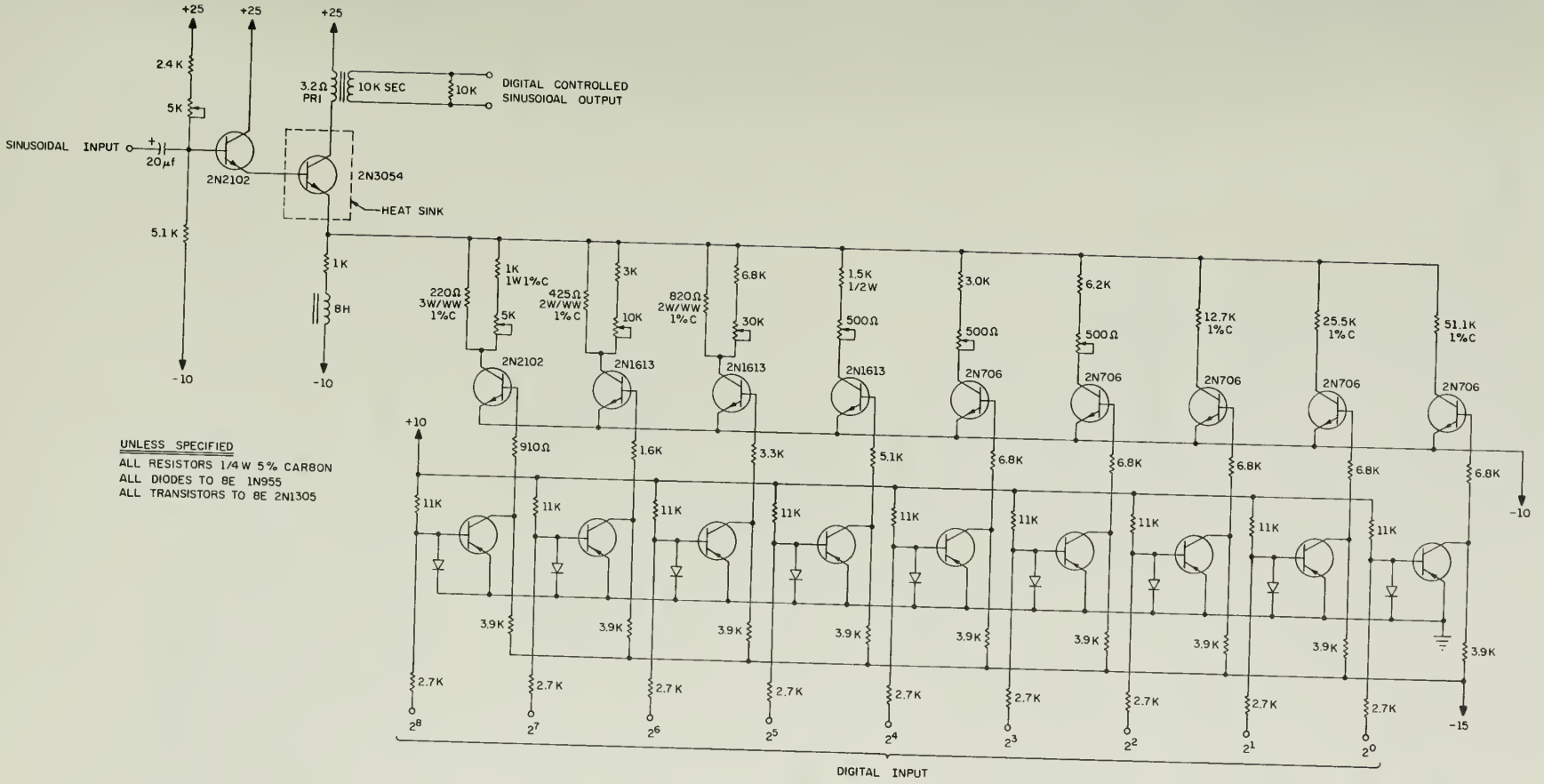


Figure A2.2 Schematic Diagram of the DCVGLA

and out of a given resistor is accomplished by a two-stage switching circuit. Two stages must be compatible with the logic levels of the digital system, and must provide the high gain needed to drive the first two most significant bits. Peak currents of the order of 200 ma flow through the transistor when switching the most significant bit. The accuracy of the system is one part in 512, or about 0.2%. A limiting condition in adding more bits is that the resistance of the least significant bit be less than the total parallel resistance of the backbiased collectors of all the other legs. In other words, the current flowing in the least significant leg must be greater than the total leadage currents in all the other legs. Another requirement is that the AC impedance in the bias drive under open circuit conditions must be large compared with the resistance of the least significant bit. The latter requirement limits the accuracy of the circuit. An inductance of 8 Hy provides an impedence of about 500K ohms compared to about 50K ohms in the path of the least significant bit.

A2.3 Integrated Circuits, 1469-103B-00, 01, 02, 03, 04.

Twelve 2-input NAND gates are mounted on the 1469-103B-00 card. These gates are contained in three Texas Instruments SN7400 integrated circuit packages, each of which is a Quad 2-input NAND gate.

Three single-phase J-K flip-flops are mounted on the 1469-103B-01 card, each of which is a Texas Instruments SN7470.

Nine 3-input NAND gates are mounted on the 1469-103B-02 card, each of which is a Texas Instruments SN7410 triple 3-input NAND gate.

Two 4-input NAND gates and two 8-input NAND gates are mounted on the 1469-103B-03 card. Component A is a Texas Instruments SN7440 or SN7420 dual 4-input NAND gate, and components B and C are Texas Instruments SN7430 8-input NAND gates.

Three monostable multivibrators are mounted on the 1469-103B-04 card, each of which is a Texas Instruments SN7380 monostable multivibrator.

A2.4 D/A CONVERTER 1469-104B

The D/A CONVERTER provides a fixed DC output voltage for a given digital input. The circuit consists of a binary chain of resistors. Each digital input switches a resistor into or out of the circuit. The currents through these resistors are then summed and amplified. The maximum conversion rate of the circuit is about 2.5 MHz. A schematic of the D/A CONVERTER is shown in Figure A2.3.

A2.5 DC and AC MIXER and AMPLIFIER 1469-105A

The DC and AC MIXER and AMPLIFIER is a digitally controlled analog circuit. The circuit performs three functions: First, it is a precision adding or subtracting circuit of DC voltages. Second, it is a compensated differential DC amplifier. Third, it is mixer which combines the DC output voltage (DC offset) of a D/A converter with a sinusoidal voltage. It can be digitally controlled to perform addition of two variable voltages, or one variable and one fixed voltage. The circuit also provides a buffered output for the hybrid PROCESSOR. Figure A2.4 shows a basic diagram of the circuit, and Figure A2.5 gives a complete schematic of the circuit. Operation of the circuit is as follows.

In the digitally controlled DC adder and subtracter, the digital control signal corresponds to either LINE or CIRCLE operation. For LINE operation, a DC voltage of the same magnitude as that of the sinusoid is added to prevent extension of the line through POINT 1. Another DC offset translates POINT 1 to the proper location on the screen. The digital signal for LINE operation selects current source I_2 in this mode. Both current source I_1 and I_2 are controlled sources. I_1 is controlled by the D/A converter which determines translation, and I_2 is controlled by the D/A converter which determines the additional DC offset required to prevent extension of the line through POINT 1. These two currents are then summed through R_s. The voltage across R_s is proportional to the sum of the currents. If one of the currents is negative with respect to a new reference, subtraction takes place.

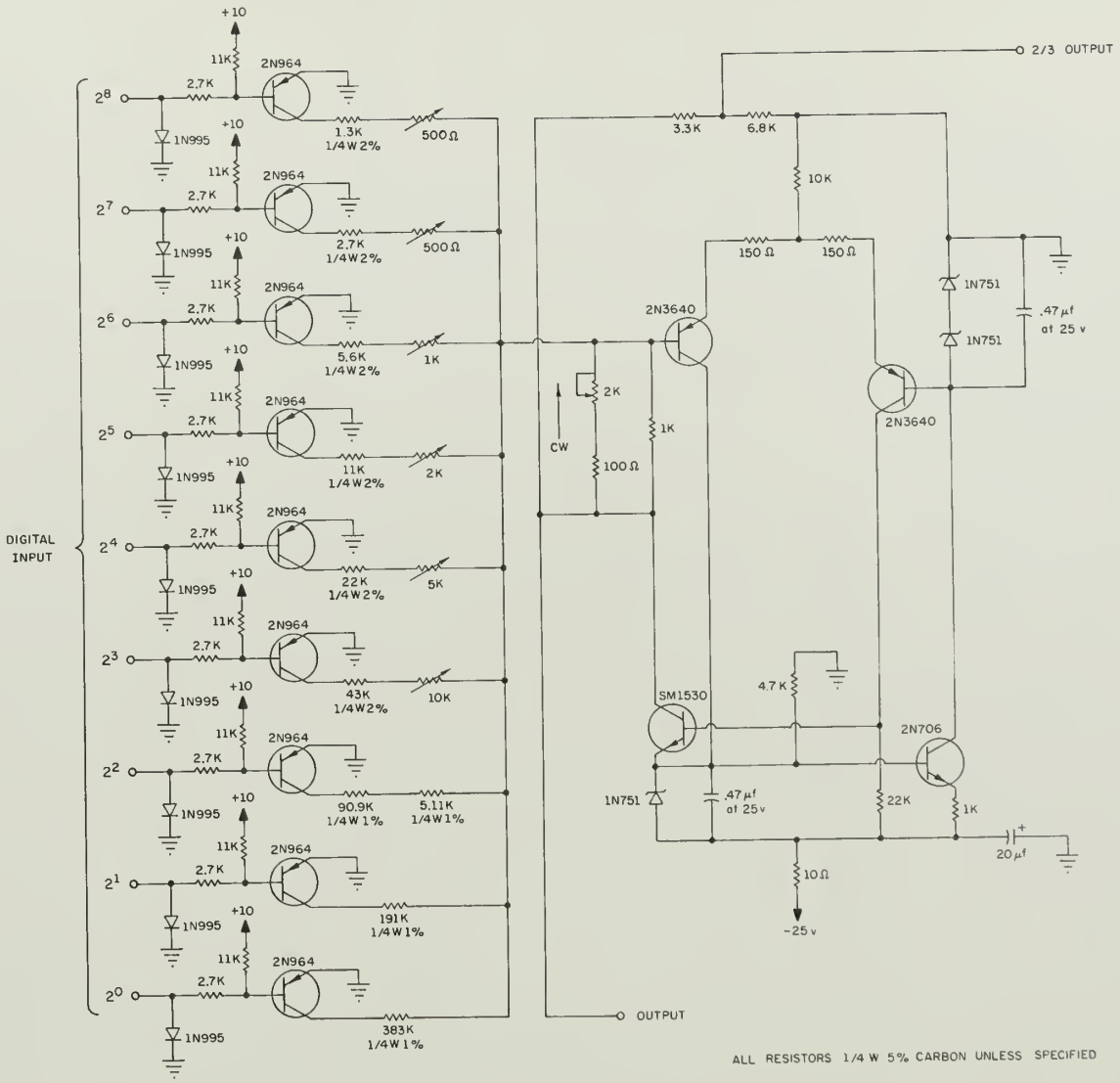


Figure A2.3 9 Bit D/A Converter

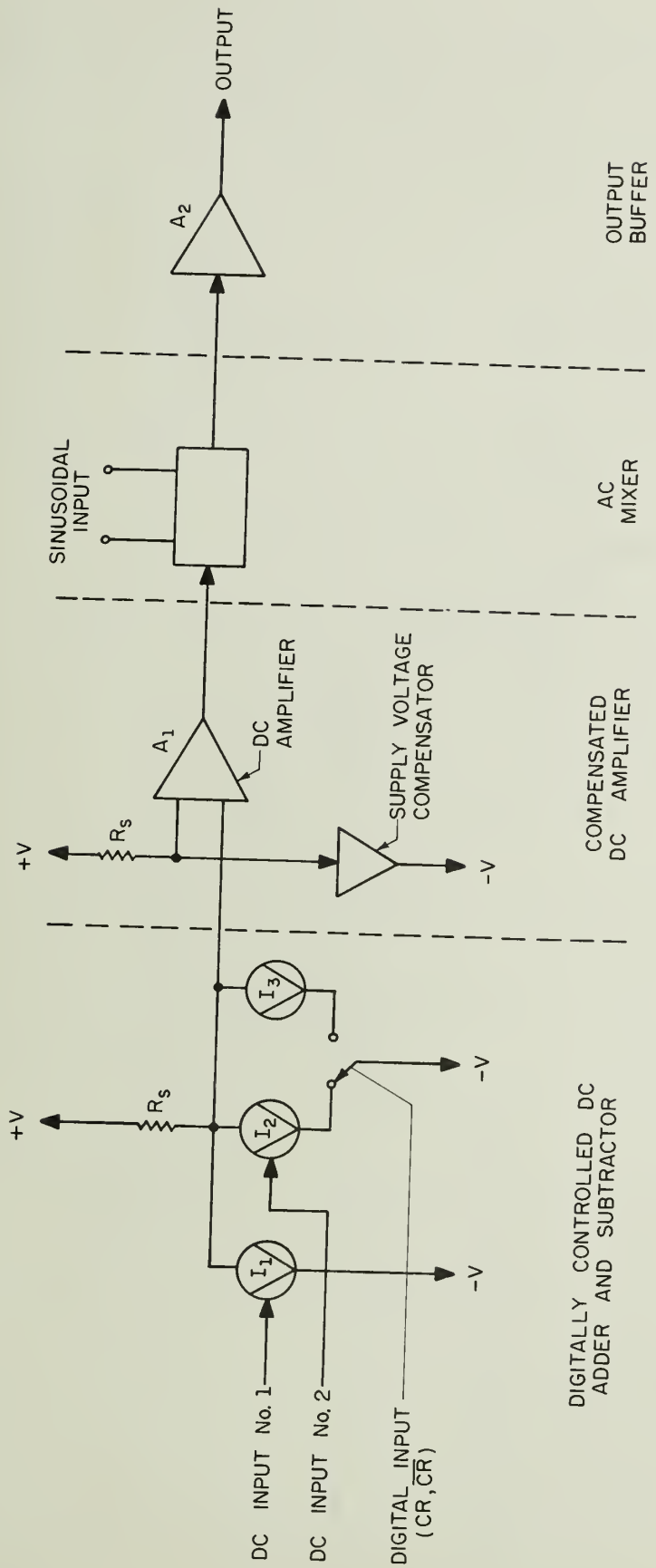


Figure A2.4 Basic Scheme of DC and AC Mixer and Amplifier

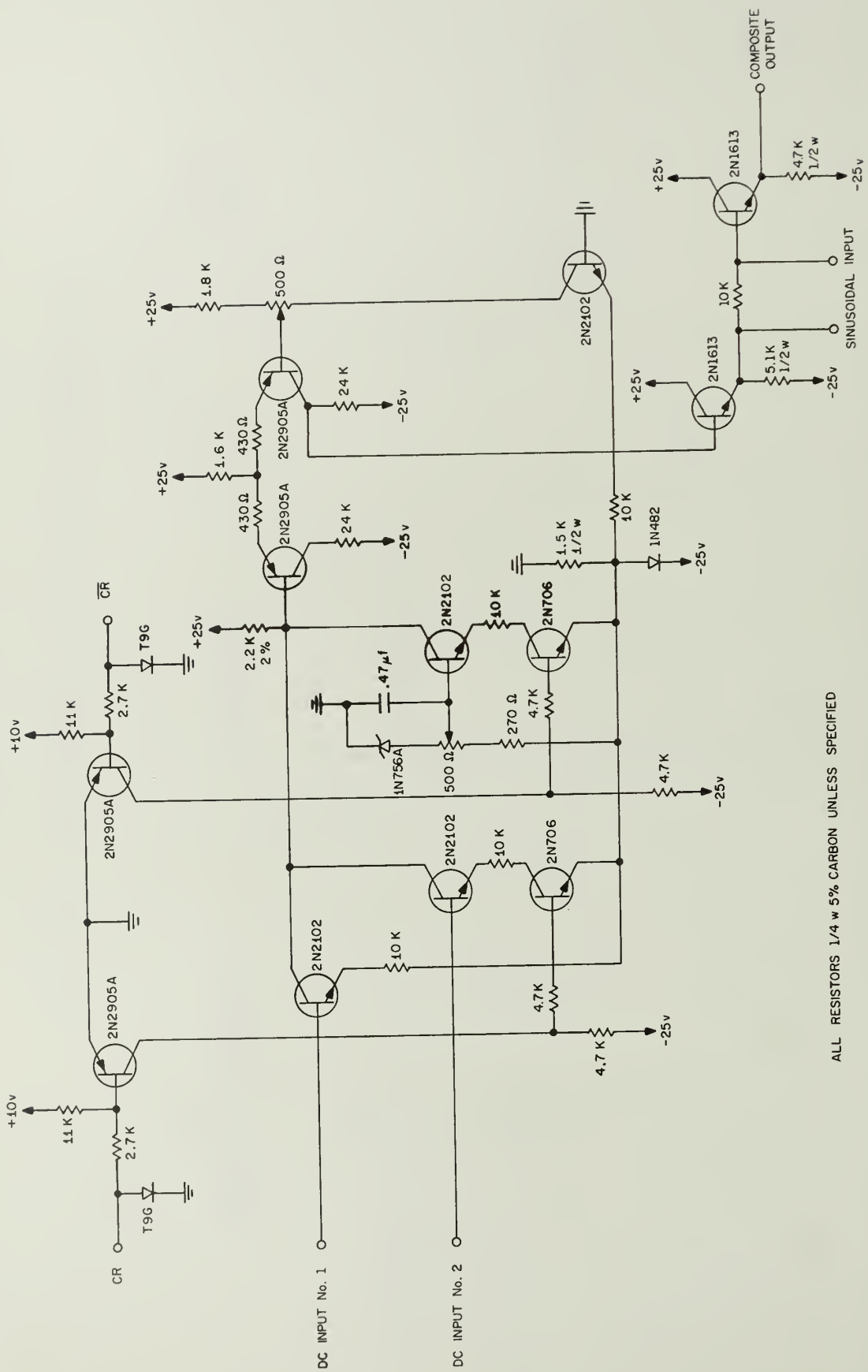


Figure A2.5 Schematic Diagram of DC and AC Mixer and Amplifier

When the system is in the CIRCLE mode of operation, the additional DC offset due to source I_2 is not used. The digital control then selects I_3, which is a fixed current source equal to the quiescent value of I_2. Since this corresponds to the zero reference, it does not cause translation of the circle. It is necessary, however, since the zero reference differs from ground or zero current at this point. This fixed current reference can be adjusted to the correct value by means of a potentiometer. The controlled current sources are essentially emitter followers, whose collector currents are summed through a 2.2K ohm resistor (R_s). The output of the adder is then applied to a compensated DC amplifier whose gain is such that a $\pm$ 10 volt variation is possible at its output. The compensation circuit was designed to prevent drift due to supply variations. The reference for the differential amplifier is essentially of the same configuration as the DC equivalent of the signal source. Hence, through common mode rejection, the supply variations are eliminated at the output.

The sinusoids are mixed with the DC voltage levels by applying the DC to an emitter follower whose output is in series with the output transformer of the DCVGLA. The AC voltage is developed by the DCVGLA across the 10K ohm resistor and is added to the DC voltage across the emitter resistor of the emitter follower. The output of this series circuit is then tied to another emitter follower, which provides a high input impedance to the mixer and a low output impedance to the rest of the system.

A2.6 DPDT RELAY, 1469-106

The DPDT RELAY circuit consists of a DPDT relay and a relay driver transistor. A grounded input causes the relay to turn on. An input of -5 volts keeps the relay off.

A2.7 DELAY MULTIVIBRATOR, 1469-107

The DELAY MULTIVIBRATOR circuit is an emitter coupled monostable multivibrator. It produces a 500 millisecond output pulse for a positive trigger input.

A2.8 CONSTANT VOLTAGE SOURCE, 1469-108

The CONSTANT VOLTAGE SOURCE circuit is part of the DCVGLA circuit and is described in section A2.2.

A2.9 8.064 MHz CLOCK 1469-109A

The 8.064 MHz CLOCK is a crystal controlled Colpitts oscillator with a two stage shaping circuit. The rise and fall times of the output pulses are less than 20 nanoseconds.

A2.10 SYNCHRONIZATION SEPARATOR, GATE DRIVER and VERTICAL BLANKING DRIVER 1469-110A

A2.10.1 SYNCHRONIZATION SEPARATOR

The SYNCHRONIZATION SEPARATOR accepts standard EIA negative composite synchronization at pin S and separates it into horizontal and vertical synchronization pulses. It also generates a logic level pulse corresponding to vertical synchronization.

The input to the SYNCHRONIZATION SEPARATOR goes through an emitter follower which drives both the horizontal and the vertical synchronization circuits. The horizontal synchronization is obtained by differentiating the output of the emitter follower. The vertical synchronization is obtained by integrating the output of the emitter follower. Both of these signals then pass to emitter followers. The outputs are at pins P and M, respectively. The output of the vertical emitter follower is integrated again in order to remove all traces of horizontal synchronization. It is then amplified and sent to an emitter follower whose output appears at pin K.

A2.10.2 GATE DRIVER

The GATE DRIVER accepts composite EIA blanking at pin D. This signal is amplified twice to raise it to the twenty volt level required by the MEMO-CORDER. Output at pin E is supplied by an emitter follower. The output signal is clipped and clamped to limit the overshoot and undershoot due to an unterminated cable.

A2.10.3 VERTICAL BLANKING LOGIC DRIVER

The VERTICAL BLANKING LOGIC DRIVER accepts the vertical blanking signal at pin F. This signal is amplified and clipped at the -5 volt level. The output at pin H is supplied by an emitter follower.

A2.11 HORIZONTAL and VERTICAL SWEEP GENERATORS, 1469-111-00 and 01

The HORIZONTAL and VERTICAL SWEEP GENERATORS supply the deflection voltages for the storage units, and are nearly identical in operation. Each consists of a synchronizing gate circuit and a linear ramp generator.

Synchronization pulses are supplied to the first stage, which gates an asymmetric astable multivibrator. The output from the multivibrator is taken at the emitter of the transistor which is cut off for the longest duration of each cycle. During this period the ramp generator supplies a linear ramp voltage whose maximum amplitude is variable from 8 to 25 volts. During the short duration of each cycle the linear sweep is discontinued by gating the ramp generator off. This produces a sawtooth voltage whose abrupt trailing edge corresponds to the retrace of the electron beams in the storage units. An astable, rather than monostable, multivibrator is employed as a safeguard in the event that the synchronization signal is lost. The beams will continue sweeping in the storage units, and not remain in a fixed position.

The ramp generator consists of an adjustable constant-current source which charges a capacitor. The generator is gated

off by discharging this capacitor at the end of each sweep. The deflection voltage is held constant while writing in the storage units by cutting off the transistor constant-current source. The emitter of the PNP transistor is held at a negative voltage with respect to the base for a period of 2 microseconds. The charging current ceases, and the voltage across the capacitor remains nearly constant during the cut-off period.

The output stage is a highly linear emitter follower which presents a relatively high impedance to the constant current source.

A2.12 ONE SHOT BUFFER, 1469-112

The ONE SHOT BUFFER circuit is an emitter coupled monostable multivibrator which generates a 2 millisecond output pulse for a positive trigger input. The 330 ohm resistor and the 0.47 μf capacitor provides filtering, if a mechanical switch is used at the input. The output of the multivibrator is amplified and clamped. Final output is supplied by emitter followers.

A2.13 VIDEO TO LOGIC CONVERTER, 1469-113

The VIDEO TO LOGIC CONVERTER is a two stage wideband amplifier with emitter follower input and output stages. It provides a -5 volt to 0-volt transition for an input between 0.5 to 2.0 volts.

A2.14 Z-AXIS DRIVER, 1469-114A

The Z-AXIS DRIVER supplies the WRITE pulses to the storage units. It supplies a negative 10-volt output pulse for any positive input pulse which exceeds 0.5 volts in amplitude. The circuit consists of an input and output emitter follower and a direct-coupled complementary NPN-PNP amplifier. The complementarity eliminates the collector delay which normally exists in the case of a

single transistor amplifier. The result is an output pulse whose rise and fall times are about 20 nanoseconds. The Z-AXIS DRIVER is regulated to accommodate 2-volt fluctuations in supply voltages.

A2.15 INDICATORS, 1469-115-03 and 04

Eight transistor drivers and eight bulbs are mounted on each INDICATOR card. The bulbs are mounted such that they are visible when the card is inserted in a card rack. The 115-03 card uses 2N1309 transistors and a 1K input resistor. The 115-04 card uses a 2N2665 transistor with a direct input.

A2.16 VIDEO ADDER and SYNCHRONIZATION INSERTER, 1469-116A

The sources of the video signals to be added may be considered as voltage sources due to the 75-ohm termination which precedes the VIDEO ADDER and SYNCHRONIZATION INSERTER circuit. The input impedance of the circuit is high relative to 75 ohms, hence there is no interaction between the video sources. The currents due to these video sources are added linearly by a resistive network, which is equipped with individual video gain controls as well as a gain control of the video sum signal. The sum is amplified by two direct-coupled amplifier stages, and the signal then proceeds to an emitter follower. Synchronization pulses which arrive at pin 17 are amplified and pull the video signal negative at the output of the emitter follower. A potentiometer adjusts the bias of the synchronization pulse amplifier, thus providing a synchronization level adjustment. The final stage of the VIDEO ADDER and SYNCHRONIZATION INSERTER circuit is a second emitter follower.

A2.17 COMPARATOR, 1469-117

The COMPARATOR compares an increasing sinusoidal voltage with a DC voltage level. The output is a 0.2 microsecond pulse which occurs when the two input voltage are within 30 millivolts of each other.

A2.18 PEN PULSE SHAPER and MULTIVIBRATOR GATE, 1469-118

The PEN PULSE SHAPER consists of a threshold amplifier followed by a second stage of amplification, and an emitter follower output stage. A tunnel diode is used at the input of the threshold amplifier and a series potentiometer selects the threshold level. The threshold amplifier acts as a discriminating circuit, adjusted to select those pulses whose amplitudes exceed the threshold.

The two amplifier stages are ac-coupled using a small differentiating capacitor to shape the incoming pulses. The output pulse width is between 50 and 100 nanoseconds.

The pulses from the PEN PULSE SHAPER trigger the MULTIVIBRATOR GATE, a monostable multivibrator followed by two current amplifiers. The outputs from these amplifiers are the SWEEP GATE pulse and the WRITE pulse, respectively.

A2.19 DISCRIMINATOR and SHAPER, 1469-119

The DISCRIMINATOR and SHAPER circuit is designed to provide shaped output voltage pulses at a fixed amplitude for any input signal which exceeds an adjustable threshold level.

The first stage is an emitter follower which buffers the input signal. The second stage amplifies this signal after which it is applied to the discrimination stage. The discrimination level is controlled by adjusting the emitter bias of this stage. The discrimination stage provides additional gain, and the output level is controlled by adjusting the amount of base drive to the final stage, the output emitter follower.

A2.20 PEN PREAMPLIFIER, 1469-121

The PEN PREAMPLIFIER circuit is designed to amplify the pulse produced by the photodiode in the LIGHT PEN. The current from the photodiode produces a voltage across its 10K load resistor. This voltage pulse is capacitively coupled into the first amplifier stage.

This stage is direct coupled to another amplifier stage which is, in turn, direct coupled to the emitter follower output stage. The switch in the circuit produces the ENABLE signal when it is closed. This switch grounds the enable line going to the pen.

A2.21 DC ADDER and AMPLIFIER

The function of this circuit is similar to that of the DC and AC MIXER and AMPLIFIER except that there is no digital control. The circuit amplifies the DC output of the 9-Bit D/A CONVERTER and mixes it with one of the sinusoidal voltages.

A2.22 General Circuit Cards, 1469-152

A2.22.1 PHASE SHIFTER and EMITTER FOLLOWER, 1469-152-00

This circuit is described in Section A2.23, 10 KHz OSCILLATOR and AMPLIFIER. It is used at the output of the oscillator to generate the sine, minus sine, and cosine voltage waveforms.

A2.22.2 AMPLIFIER and EMITTER FOLLOWER, 1469-152-01

The AMPLIFIER and EMITTER FOLLOWER circuit amplifies the incoming signal, clamps it to a -5 volts, and provides a buffered output. It is designed to restore a signal to logic levels.

A2.22.3 10 KHz SQUARE WAVE GENERATOR, 1469-152-02

This circuit provides a 10 KHz square wave at its output, pin 19, when a 10KHz sine wave is applied to the input, pin C.

A2.22.4 +1.7 VOLT POWER SUPPLY, 1469-152-03

The +1.7 VOLT POWER SUPPLY generates +1.7 volts from a +10 volt input level.

A2.22.5 EMITTER FOLLOWER, 1469-152-04

The EMITTER FOLLOWER circuit amplifies the input, clamps it at -5 volts, and provides a buffered output.

A2.22.6 EMITTER FOLLOWERS, 1469-152-05

Emitter Followers A and B on card 152-05 are coaxial cable drivers which buffer the integrated circuits. Circuit C is designed to drive the display monitor directly. Its input is the cross-hatch grid generated by the processor intregrated circuits. Circuit D is used to shift the level of the composite synchronization signal, generated by the CAMERA CONTROL UNIT, to that of the integrated circuits in the PROCESSOR.

A2.22.7 PEN GATE, 1469-152-06

The PEN GATE circuit is a collector coupled monostable multivibrator which generates a 200 μ second output pulse for a positive trigger pulse input. The output is buffered by an emitter follower.

A2.23 PLUS and MINUS SINE and COSINE GENERATOR, 1469-153-00

The circuit consists of four sections: a sinusoisal oscillator, an amplifier, a phase-shifting network, and an output buffer network with amplitude control of each sinusoid. A schematic diagram of the circuit is given in Figure A2.6.

The oscillator is a Colpitts configuration with emitter feedback. Since frequency stability is of no consequence, a free-running LC tuned configuration proved adequate. The loop-gain is adjusted as close as possible to unity to provide the greatest linearity. A frequency of 10KHz is used so as not to exceed the response time of the ARTRIX COMPARATOR circuit. Also, at this frequency any third harmonic distortion does not pass through transformer used in the phase-shifting network and the DCVGLA. The amplfier is a single ended class A configuration with a transformer output. The only caution to be observed is that of not saturating the transformer. This

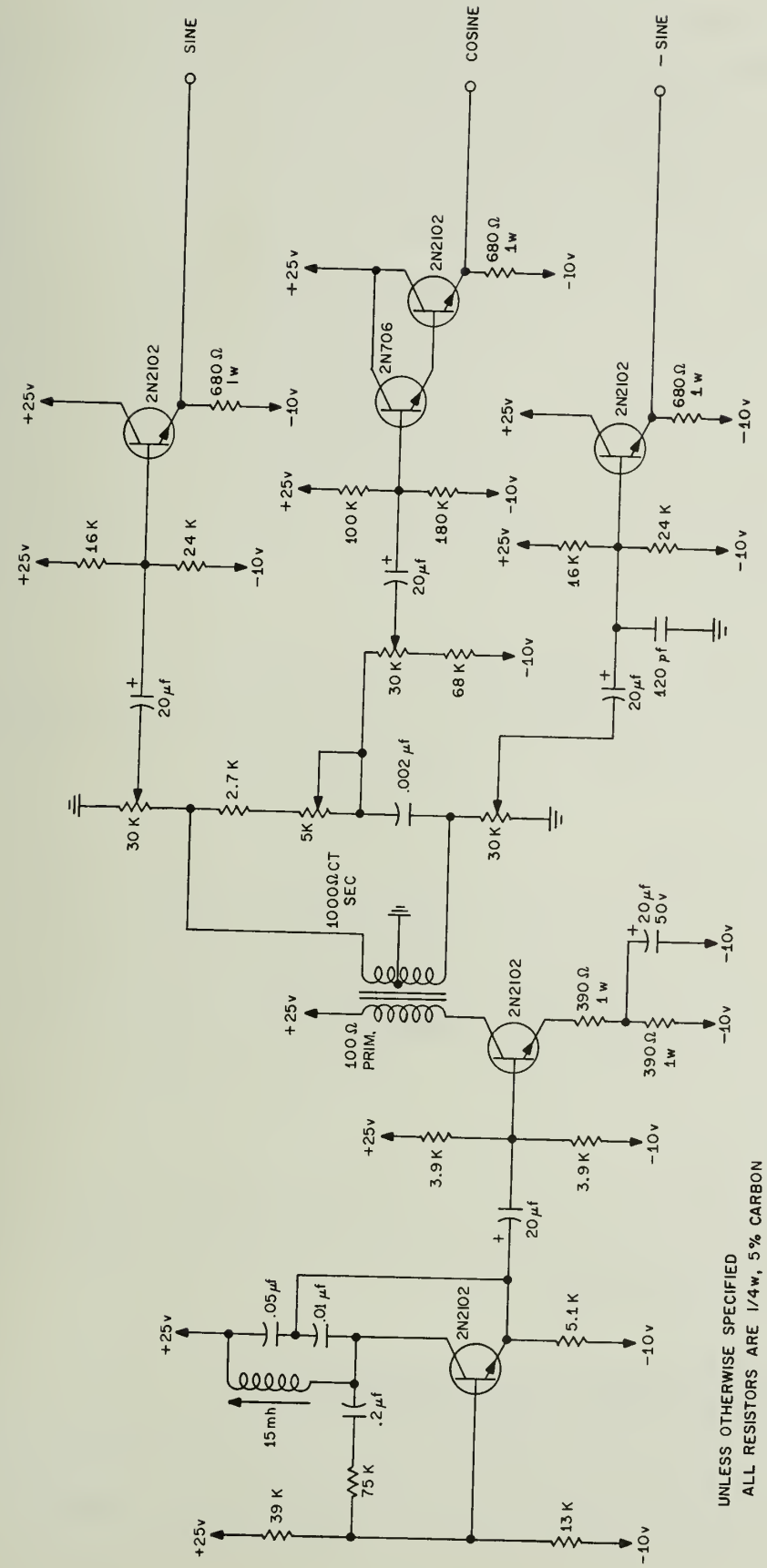


Figure A2.6 Schematic of PLUS and MINUS SINE and COSINE GENERATOR

transformer also serves as the heart of the phase-shfiting network. By grounding the center tap of the transformer, the signals at the two ends of the winding are 180 degrees out of phase. These provide positive and negative sinusoidal functions. By placing a resistor R and a capacitor C, whose reactance at 10KHz is equal in magnitude to R, across the transformer, one can obtain a signal exactly 90 degrees out of phase with either end of the transformer. This signal then provides the cosine function. Since R is variable, the phase of the cosine function can be adjusted independently of the other signals. The outputs of the transformer and phase-shift network are controlled by potentiometers and fed to emitter followers to provide a buffer for the next stage. A Darlington configuration is used for the cosine function since its phase stability is more dependent on the input impedence into the emitter follower. The circuit exhibits excellent linearity.

A2.24 VOLTAGE MONITOR, 1469-157

This circuit is described in the discussion of the VOLTAGE MONITOR. See Section A1.3.

A2.25 Hg RELAY, 1469-164

The Hg RELAY circuit is a mercury wetted relay and driver with a diode OR logic input. There are 3 diode OR inputs on each relay and a common input for the whole card. In addition, there is an output from the driver transistors and a diode input which goes directly to the relay.

A2.26 FILTER, 1469-173

The circuit consists of 18 independent switch filters. The outputs are at about -5 volts when the inputs are open and near ground when the inputs are at ground.

A2.27 PEN EMITTER FOLLOWER and ENABLE FILTER

This circuit is an emitter follower which provides a low output impedance for driving a cable with the LIGHT PEN pulse. Noise generated at the ENABLE switch in the LIGHT PEN is eliminated by the ENABLE FILTER.

A3.0 Complete ARTRIX Drawings

A3.1 System Drawings

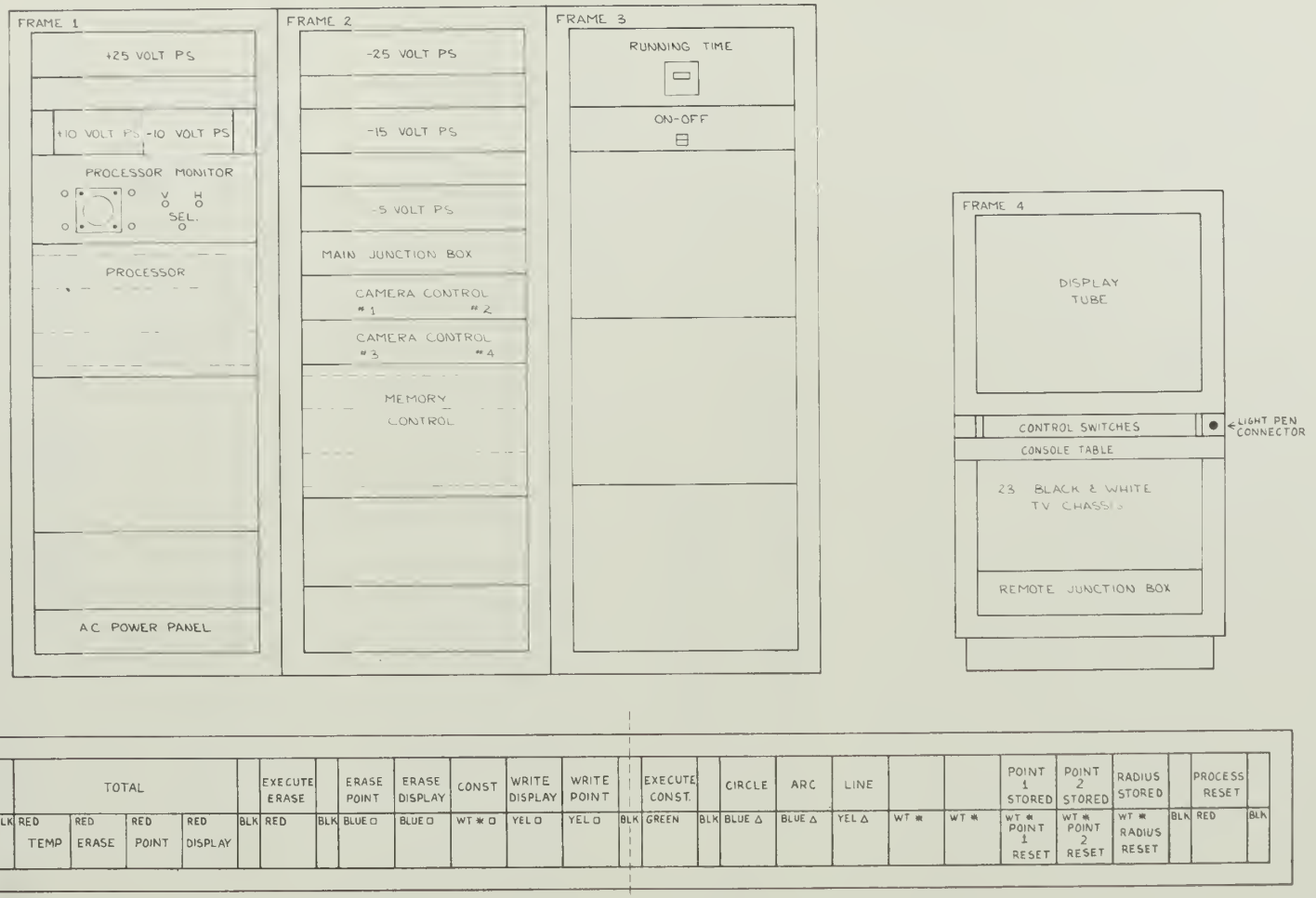


Figure 3.1.1 Panel Layout

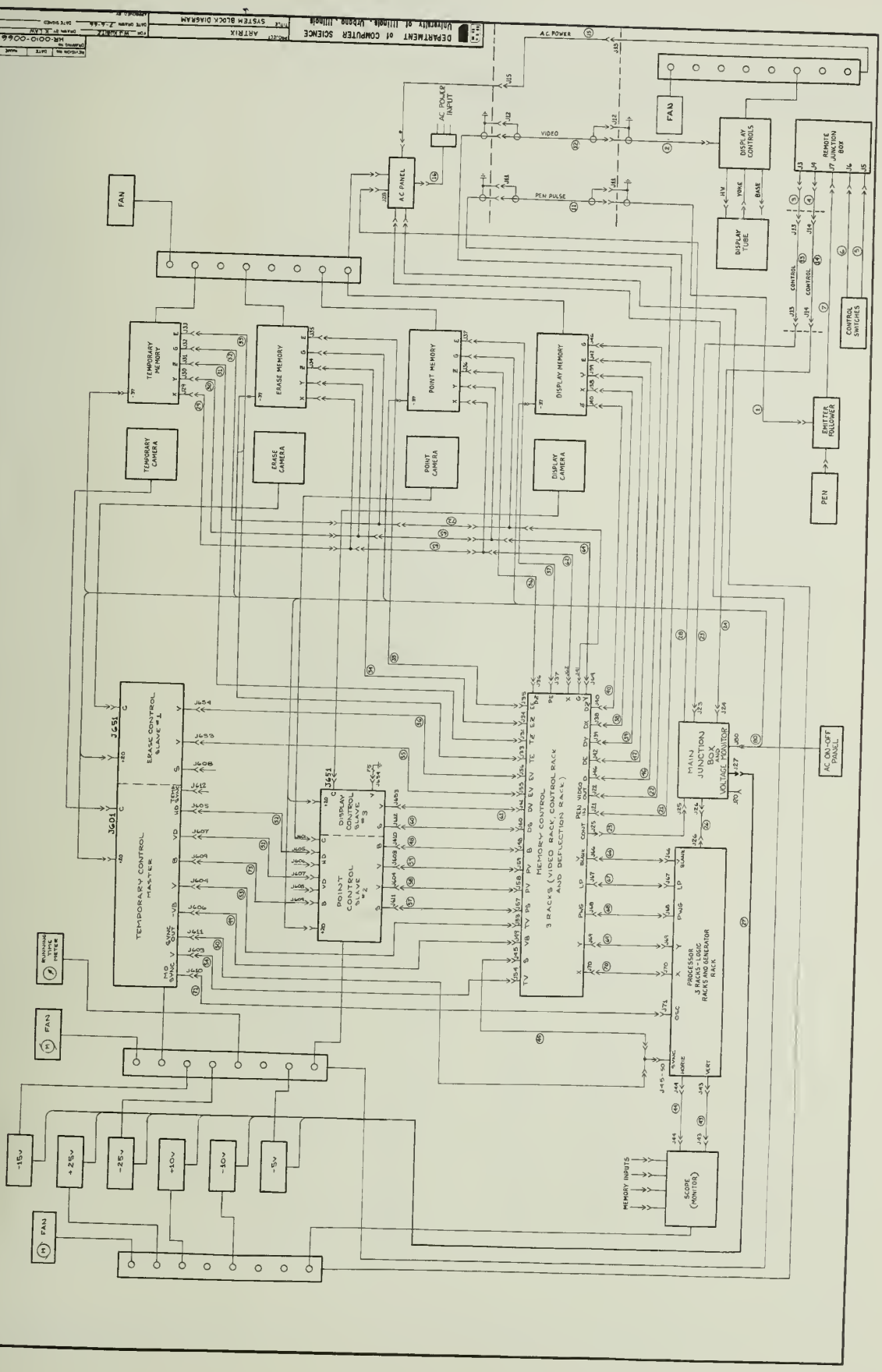


Figure A3.1.2 System Block Diagram

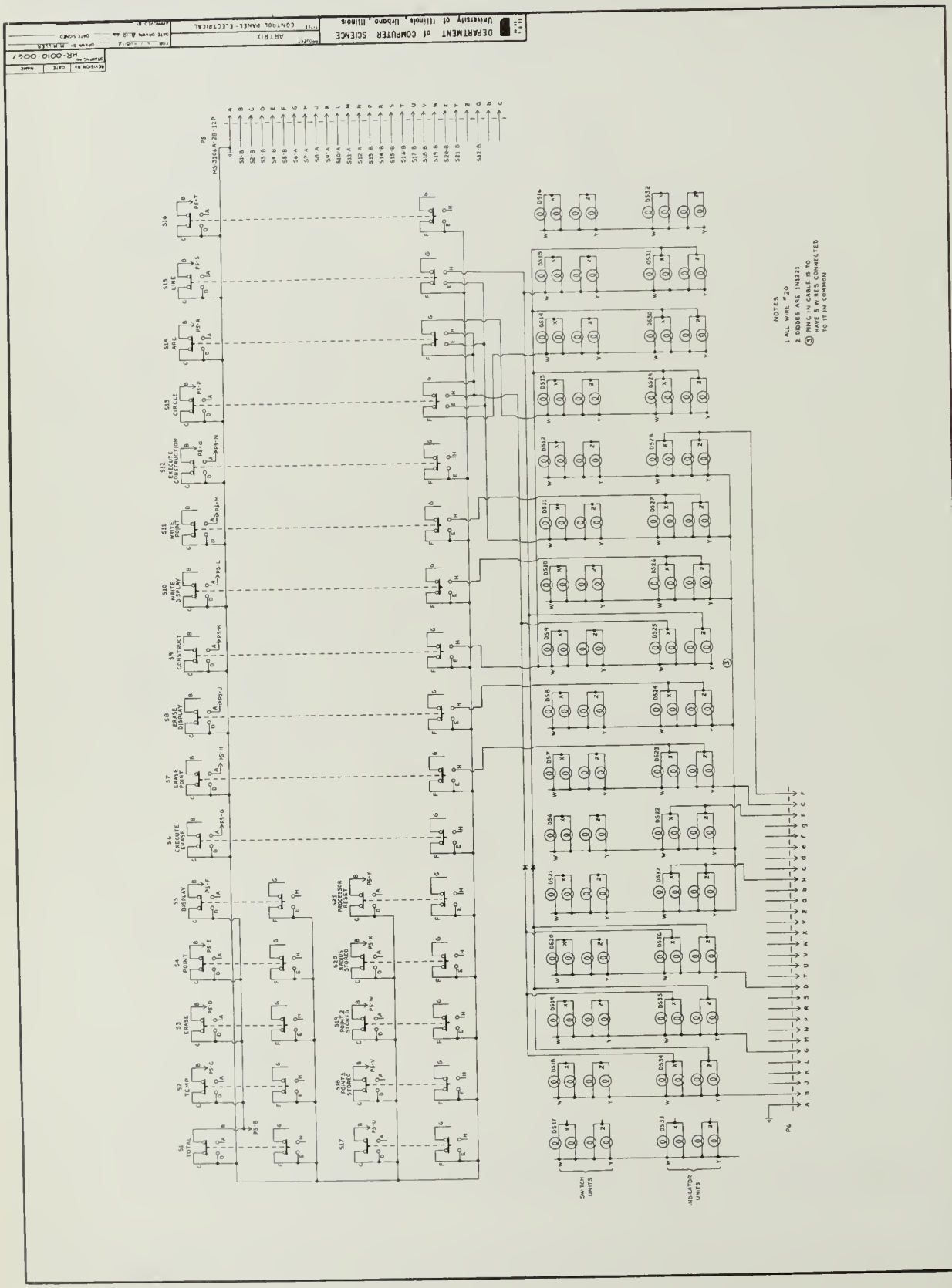


Figure A3.1.3 Control Panel

A3.1.4 LIGHT PEN

See Sec. A3.4, 1469-121 P.C. Board

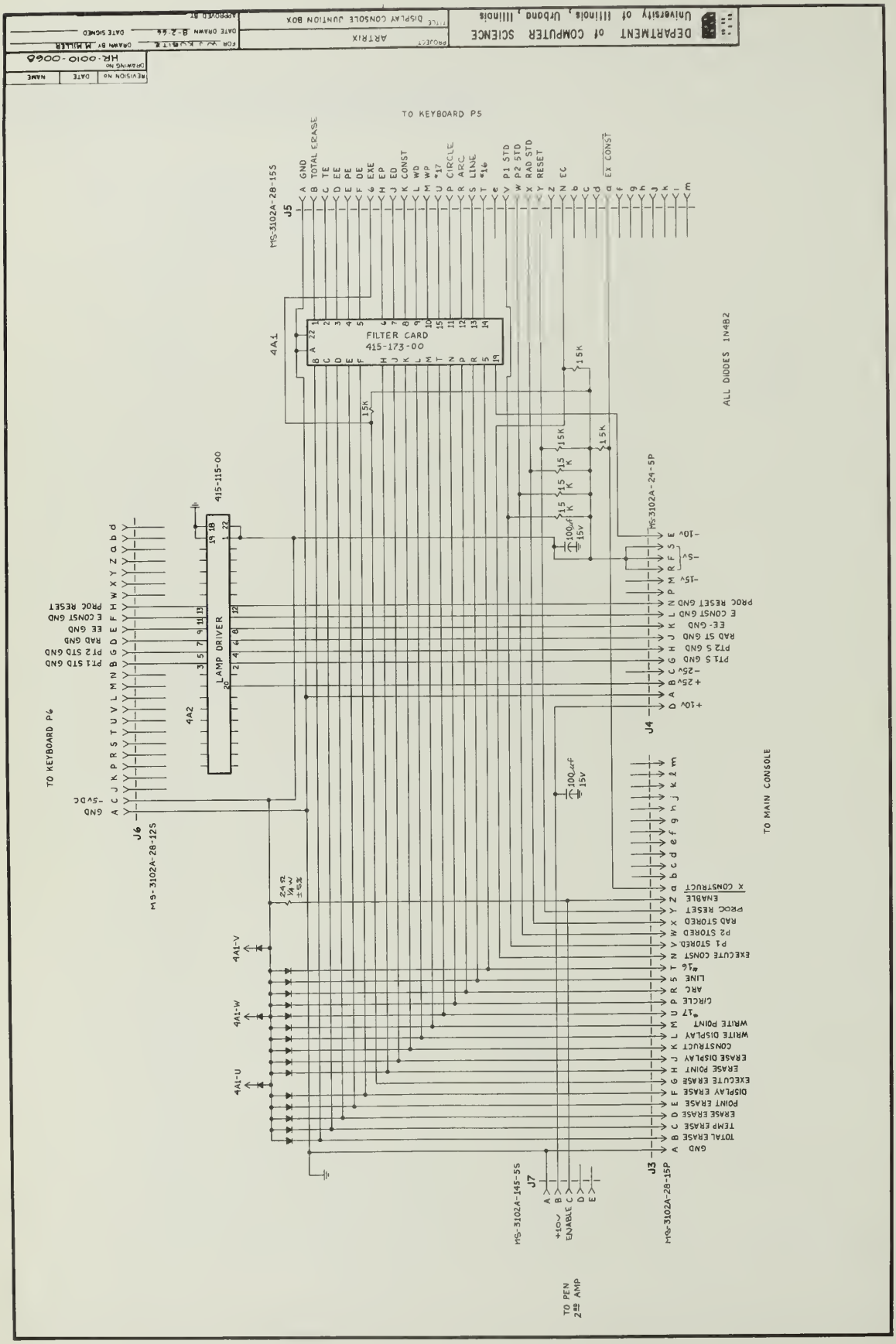


Figure A3.1.5 DISPLAY CONSOLE JUNCTION BOX

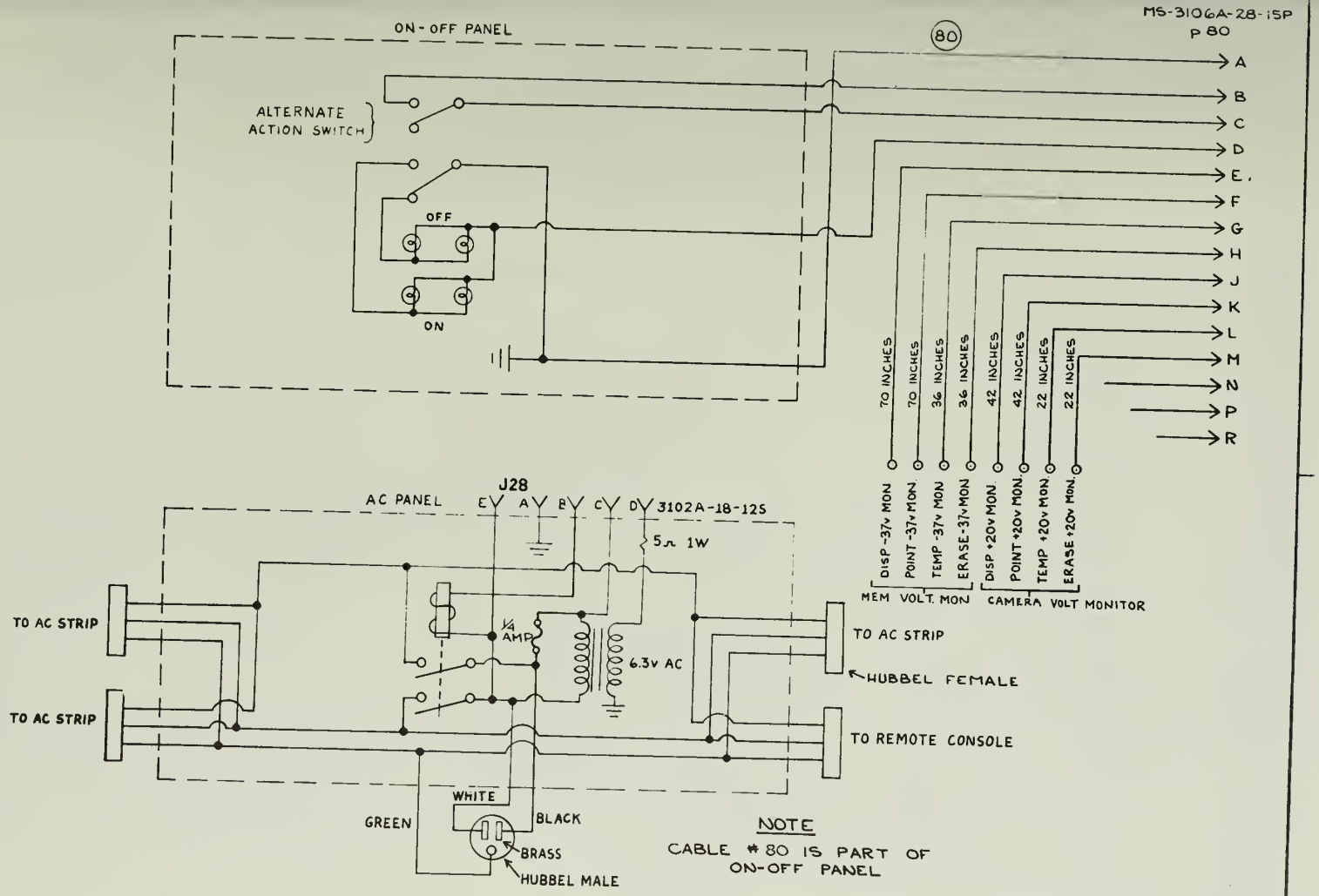


Figure A3.1.6 AC PANEL and AC ON-OFF PANEL

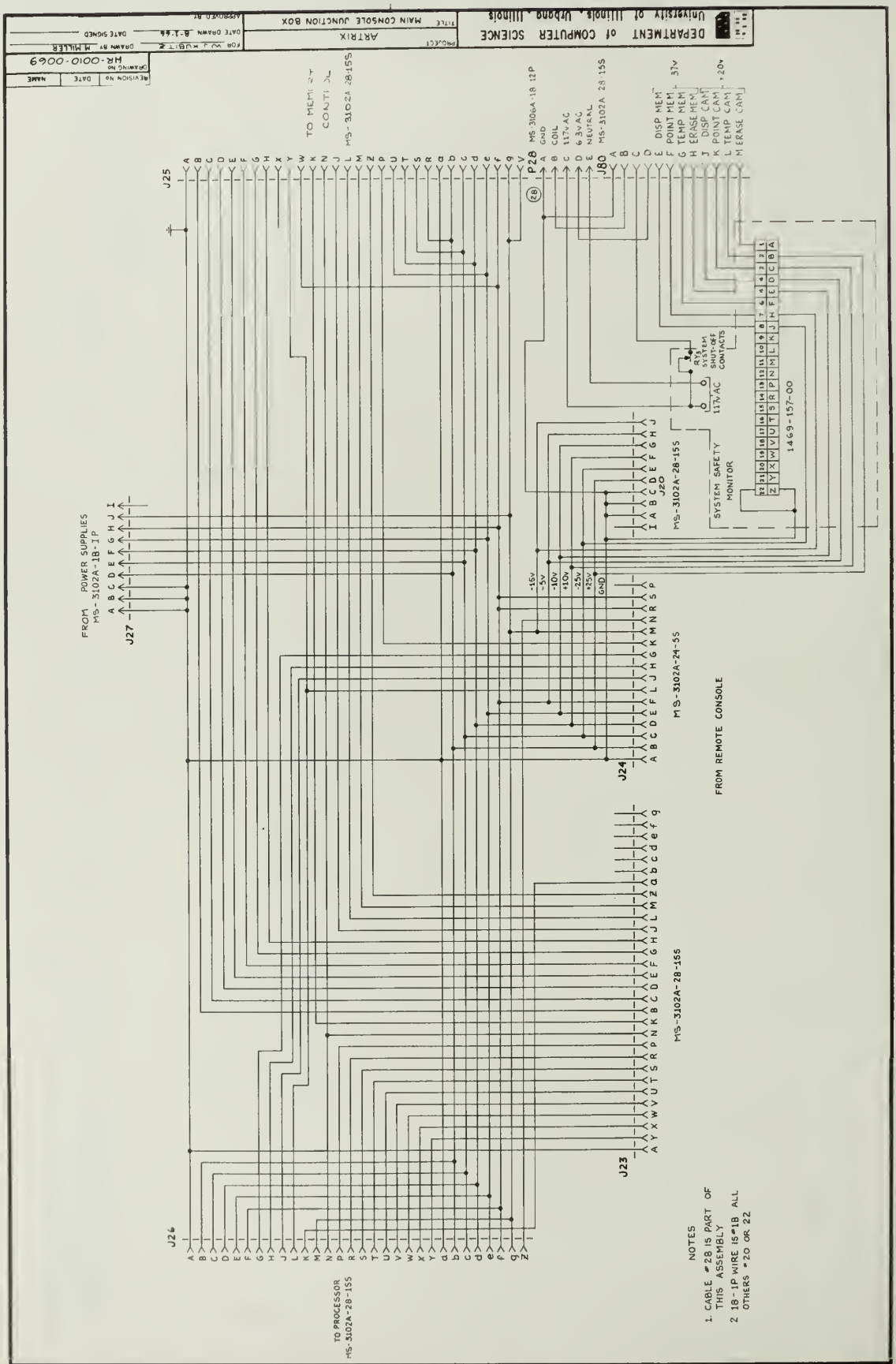


Figure A3.1.7 MAIN CONSOLE JUNCTION BOX

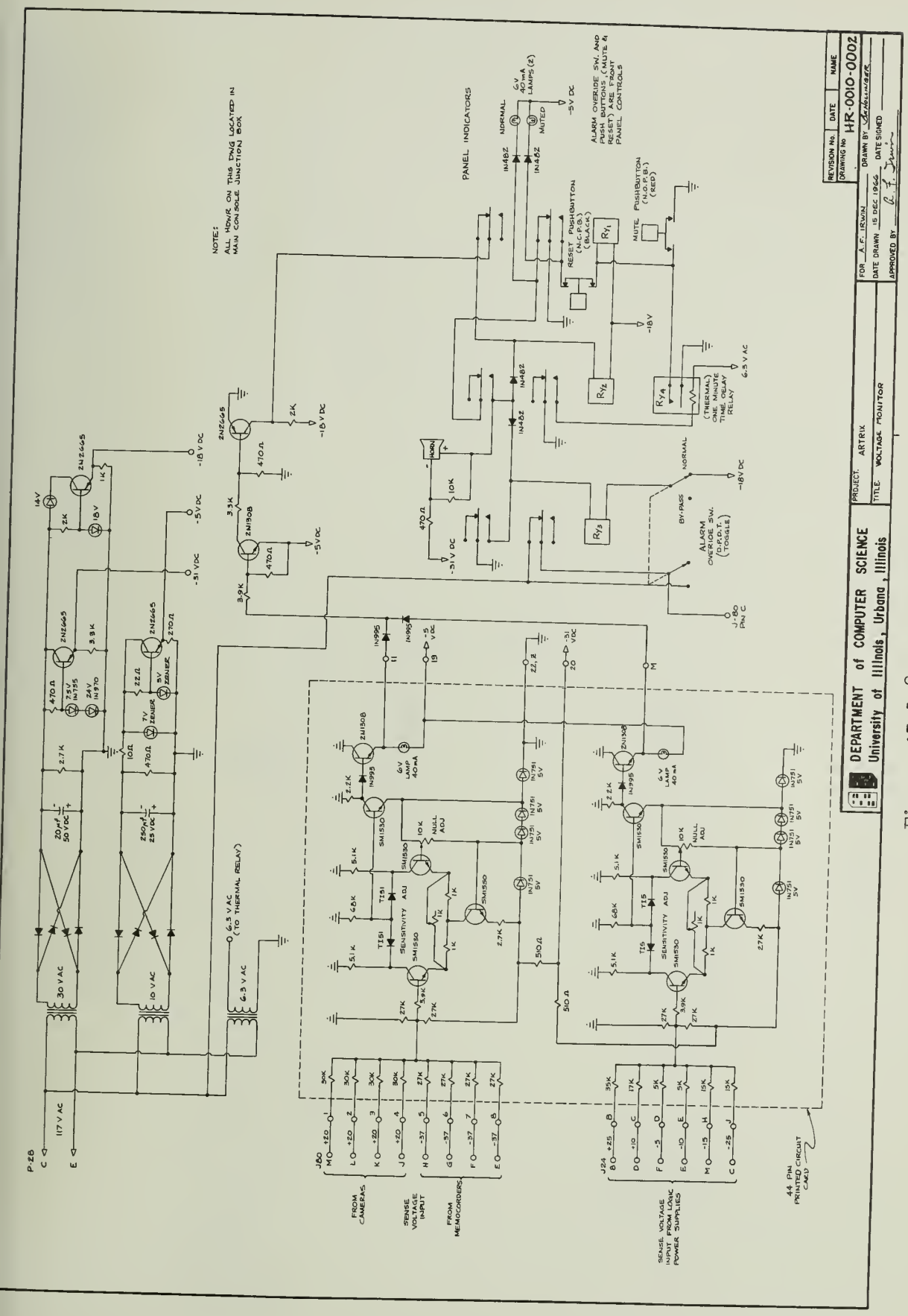
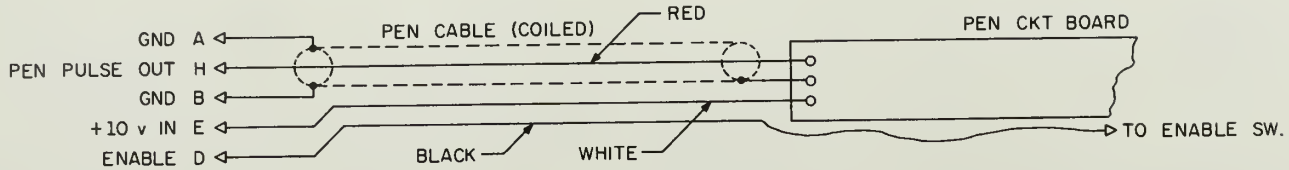


Figure A3.1.8 VOLTAGE MONITOR

ARTRIX PEN CABLE DIAGRAM



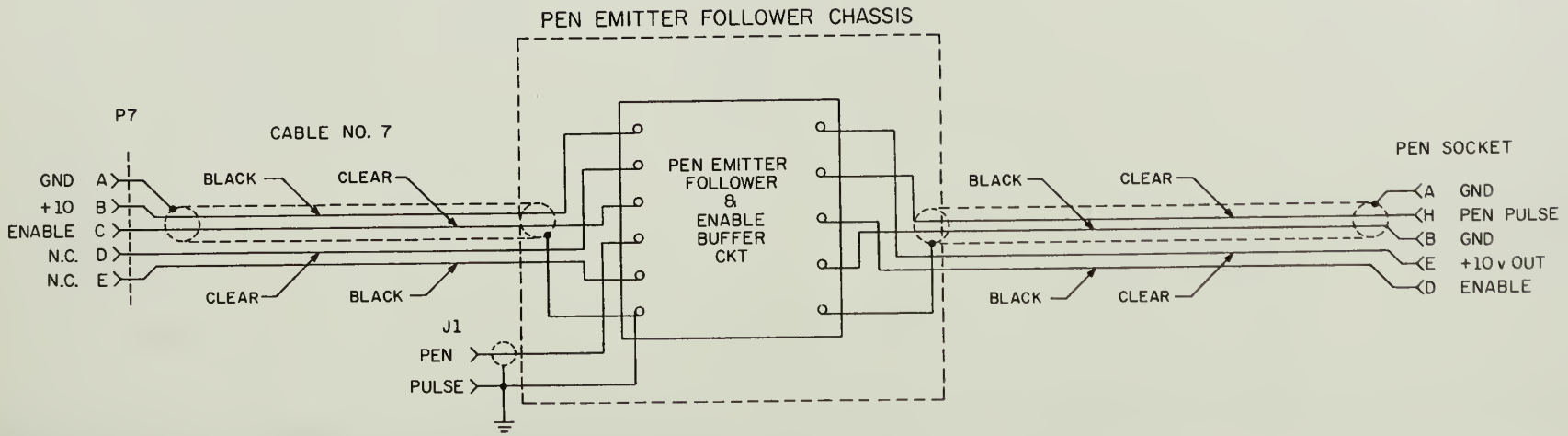


Figure A3.1.9

A3.2.0 Memory Drawings

A3.2.1 MEMORY CONTROL Card Rack List

RACK A

SPACE	NUMBER	NAME
1	1469-118A-00	PEN PULSE SHAPING CIRCUIT and MULTIVIBRATOR GATE
2	1469- 14A-00	DIAMOND GATE
3	1469- 14A-00	DIAMOND GATE
4	1469-113A-00	VIDEO to LOGIC CONVERTER
5	1469-114A-00	Z-AXIS DRIVER
6	1469-114A-00	Z-AXIS DRIVER
7	1469-116A-00	VIDEO ADDER/SYNCHRONIZATION INSERTER
8	1469-118A-00	VIDEO ADDER/SYNCHRONIZATION INSERTER
9	1469-152 -04	EMITTER FOLLOWER
10	1469-152 -03	+1.7 VOLT POWER SUPPLY
11	1469-152 -06	PEN GATE MULTIVIBRATOR
12	1469-119 -00	DISCRIMINATOR and SHAPER
13	1469-119 -00	DISCRIMINATOR and SHAPER
14	1469-119 -00	DISCRIMINATOR and SHAPER
15	1469-119 -00	DISCRIMINATOR and SHAPER

RACK B

SPACE	NUMBER	NAME
1	1469-115 -03	INDICATOR
2	1469-112 -00	ONE SHOT BUFFER
3	1469-103B-00	2-Input NAND
4	1469-103B-00	2-Input NAND
5	1469-103B-00	2-Input NAND
6	1469-103B-01	J-K Flip-Flop
7	1469-103B-01	J-K Flip-Flop
8	1469-103B-02	3-Input NAND
9	1469-115B-03	INDICATOR
10	1469-103B-00	2-Input NAND
11	1469-107 -00	RELAY GATE
12	1469-103B-00	2-Input NAND
13	1469-164B-00	MERCURY RELAY
14	----	----
15	1469-173 -00	FILTER
16	1469-152 -01	Emitter Follower

RACK C

SPACE	NUMBER	NAME
1	1469-110A-00	SYNCHRONIZATION SEPARATOR/GATE DRIVER/VERTICAL BLANKING LOGIC DRIVER
2	1469-111A-00	VERTICAL SWEEP GENERATOR
3	1469-111A-01	HORIZONTAL SWEEP GENERATOR
4	1469-106 -00	DPDT RELAY
5	----	----
6	1469-152 -07	DISPLAY GATE GENERATOR

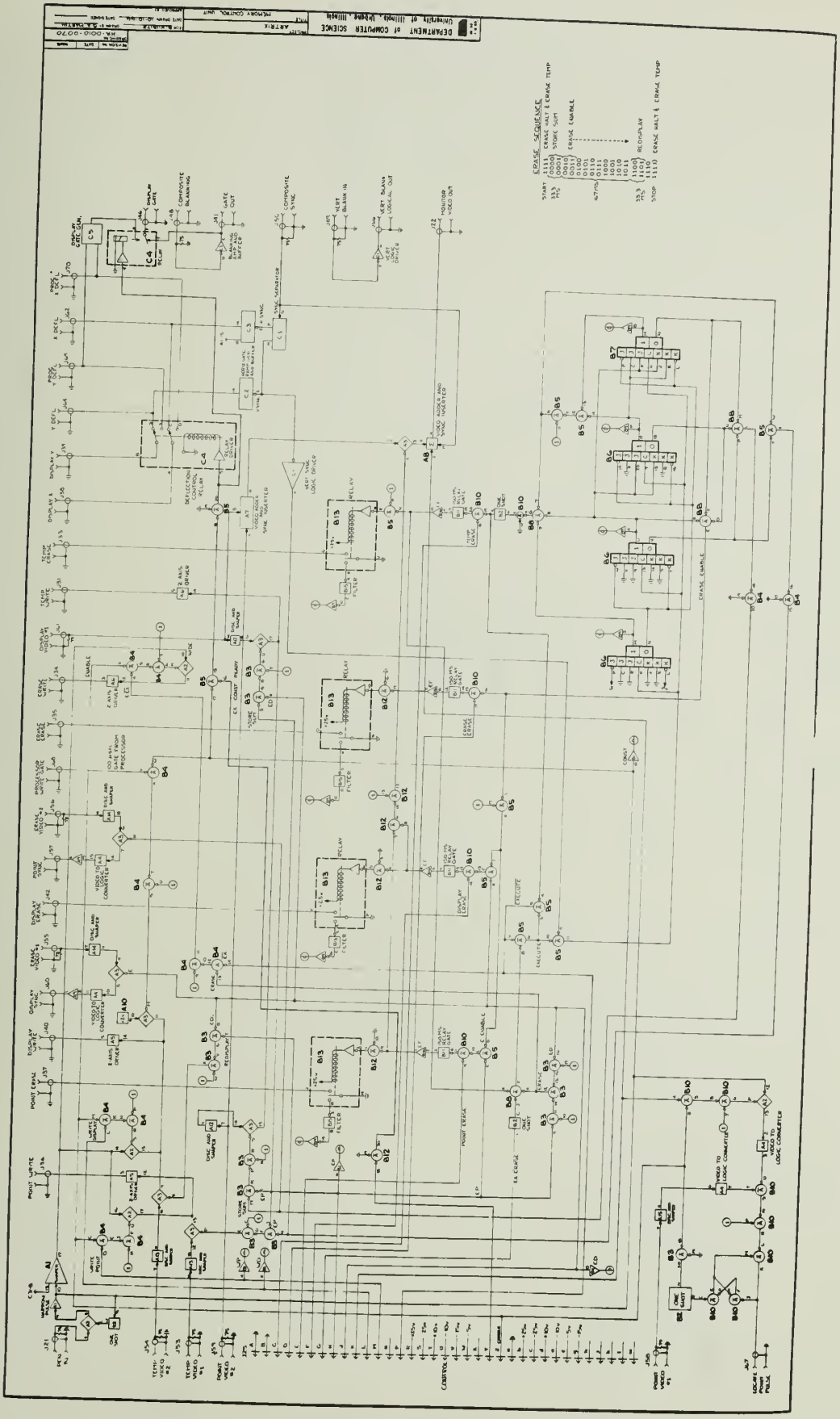
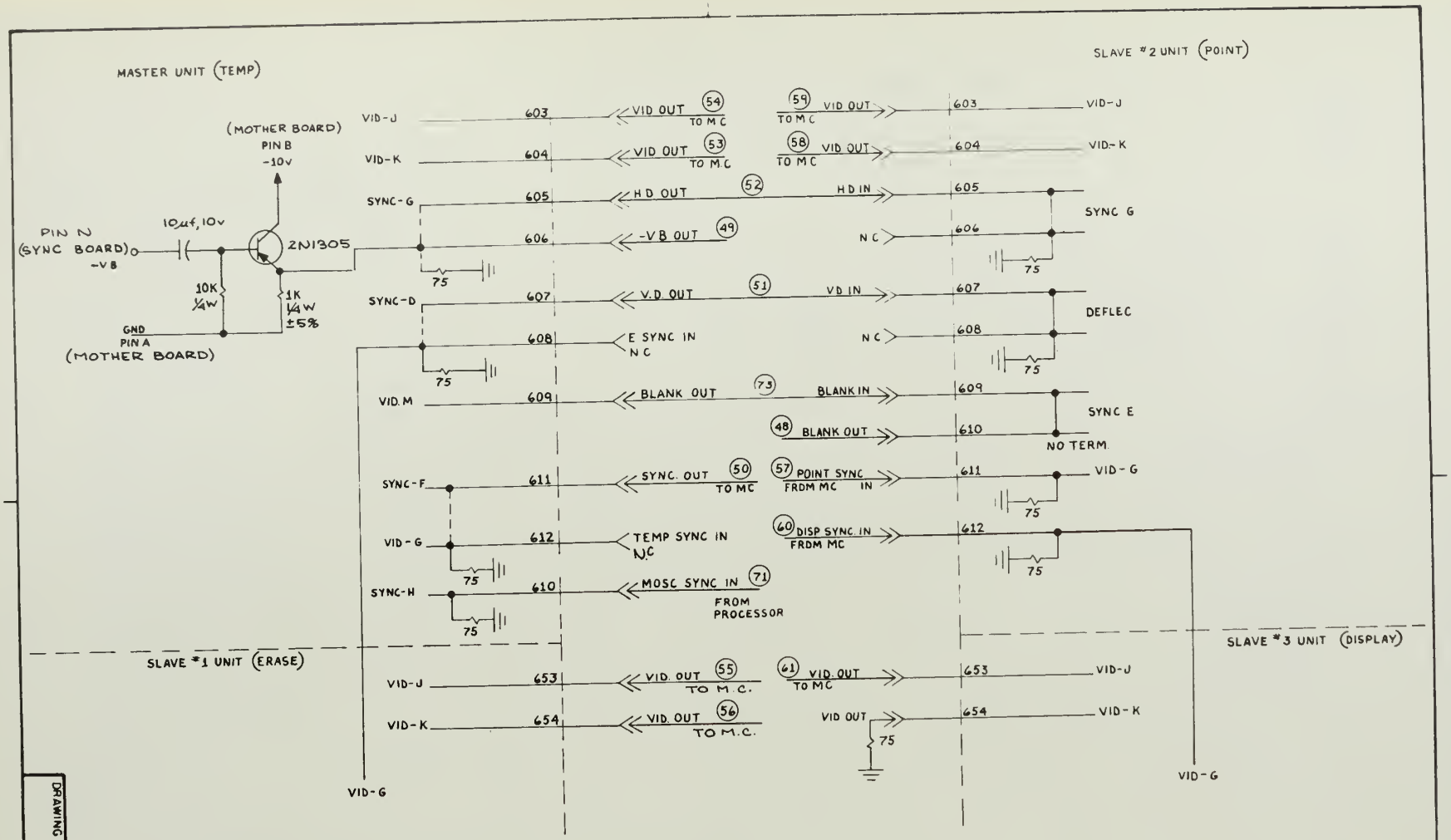


Figure A3.2.2 MEMORY CONTROL UNIT



NOTES

3. VID-J = VIDEO PLUG-IN CIRCUIT BOARD, PIN J.
2. M.C. = MEMORY CONTROL UNIT.
1. DOTTED LINES INDICATE CONNECTIONS WHICH HAVE BEEN REMOVED

DRAWING No

REVISION No	DATE	NAME
DRAWING No HR-0010-0071		

DEPARTMENT of COMPUTER SCIENCE
University of Illinois, Urbana, Illinois

PROJECT ARTRIX

TITLE PARTIAL SCHEMATIC SHOWING MODIFICATIONS TO COHU CAMERA CONTROL UNITS

FOR W.J. KUBITZ DRAWN BY M. MILLER

DATE DRAWN 8-4-66 DATE SIGNED

APPROVED BY

Figure A3.2.3 PARTIAL SCHEMATIC of CAMERA CONTROL UNIT

A3.3.0 PROCESSOR Drawings

A3.3.1 PROCESSOR Card Rack List

RACK A

CARD TYPE	VARIATION	FUNCTION
1. 103B	00	2-Input NAND
2. 103B	00	2-Input NAND
3. 103B	00	2-Input NAND
4. 103B	00	2-Input NAND
5. 103B	00	2-Input NAND
6. 103B	02	3-Input NAND
7. 103B	01	J-K Flip-Flop
8. 103B	03	4 and 8-Input NAND
9. 103B	01	J-K Flip-Flop
10. 103B	01	J-K Flip-Flop
11. 103B	03	4 and 8-Input NAND
12. 103B	01	J-K Flip-Flop
13. 103B	03	4 and 8-Input NAND
14. 103B	01	J-K Flip-Flop
15. 103B	01	J-K Flip-Flop
16. 103B	01	J-K Flip-Flop
17. 103B	03	4 and 8-Input NAND
18. 103B	01	J-K Flip-Flop
19. 103B	01	J-K Flip-Flop
20. 103B	01	J-K Flip-Flop
21. 103B	01	J-K Flip-Flop
22. 103B	01	J-K Flip-Flop
23. 103B	01	J-K Flip-Flop
24. 103B	01	J-K Flip-Flop
25. 103B	01	J-K Flip-Flop
26. 103B	01	J-K Flip-Flop
27. 103B	01	J-K Flip-Flop
28. 103B	01	J-K Flip-Flop

RACK B

TYPE	VARIATION	FUNCTION
1. 103B	01	J-K Flip-Flop
2. 103B	01	J-K Flip-Flop
3. 103B	01	J-K Flip-Flop
4. 103B	00	2-Input NAND
5. 103B	00	2-Input NAND
6. 103B	00	2-Input NAND
7. 103B	02	3-Input NAND
8. 103B	00	2-Input NAND
9. 103B	02	3-Input NAND
10. 103B	00	2-Input NAND
11. 115B	03	INDICATOR
12. 115B	03	INDICATOR
13. 115B	03	INDICATOR
14. 103B	00	2-Input NAND
15. 115B	03	INDICATOR
16. 115B	03	INDICATOR
17. 115B	03	INDICATOR
18. 103B	00	2-Input NAND
19. 115B	03	INDICATOR
20. 115B	03	INDICATOR
21. 115B	03	INDICATOR
22. 103B	02	3-Input NAND
23. 115B	03	INDICATOR
24. 103B	01	J-K Flip-Flop
25. 103B	03	4 and 8-Input NAND
26. 103B	04	MONOSTABLE MULTIVIBRATOR
27. 104B	00	9 BIT D/A CONVERTER
28. 152	05	EMITTER FOLLOWER

RACK C

TYPE	VARIATION	FUNCTION
1. 153	00	10 KHz OSCILLATOR and AMPLIFIER
2. Blank	--	----
3. Blank	--	----
4. 152	--	PHASE SHIFTER and EMITTER FOLLOWER
5. 106	00	DPDT RELAY
6. Blank	--	----
7. 108	00	CONSTANT VOLTAGE SOURCE
8. Blank	--	----
9. Blank	--	----
10. Blank	--	----
11. 102B	00	DCVGLA
12. 108	00	CONSTANT VOLTAGE SOURCE
13. Blank	--	----
14. Blank	--	----
15. Blank	--	----
16. 102B	00	DCVGLA
17. 123	00	DC and AC ADDER and AMPLIFIER
18. 104B	00	9 BIT D/A CONVERTER
19. 104B	00	9 BIT D/A CONVERTER
20. 152	02	10KHz SQUARE WAVE GENERATOR
21. 104B	00	9 BIT D/A CONVERTER
22. 104B	00	9 BIT D/A CONVERTER
23. 105A	00	D.C. AMPLIFIER and MIXER
24. 117	00	COMPARATOR
25. 117	00	COMPARATOR
26. 109A	00	8.064 MHz CLOCK
27. 104B	00	9 BIT D/A CONVERTER
28. 104B	00	9 BIT D/A CONVERTER

A3.3.2 Digital Section

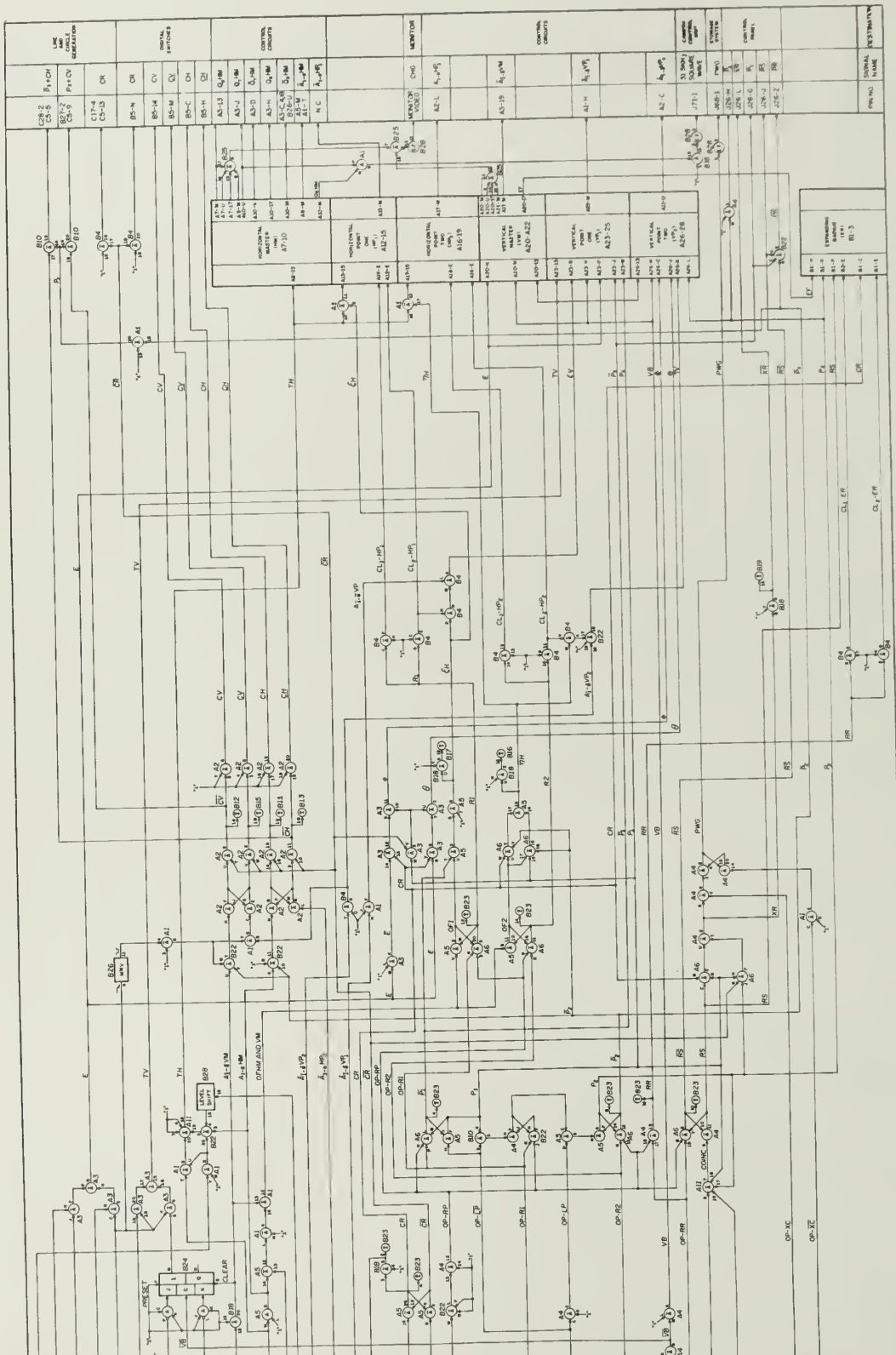


Figure A3.3.2.1 PROCESSOR CONTROL Circuits

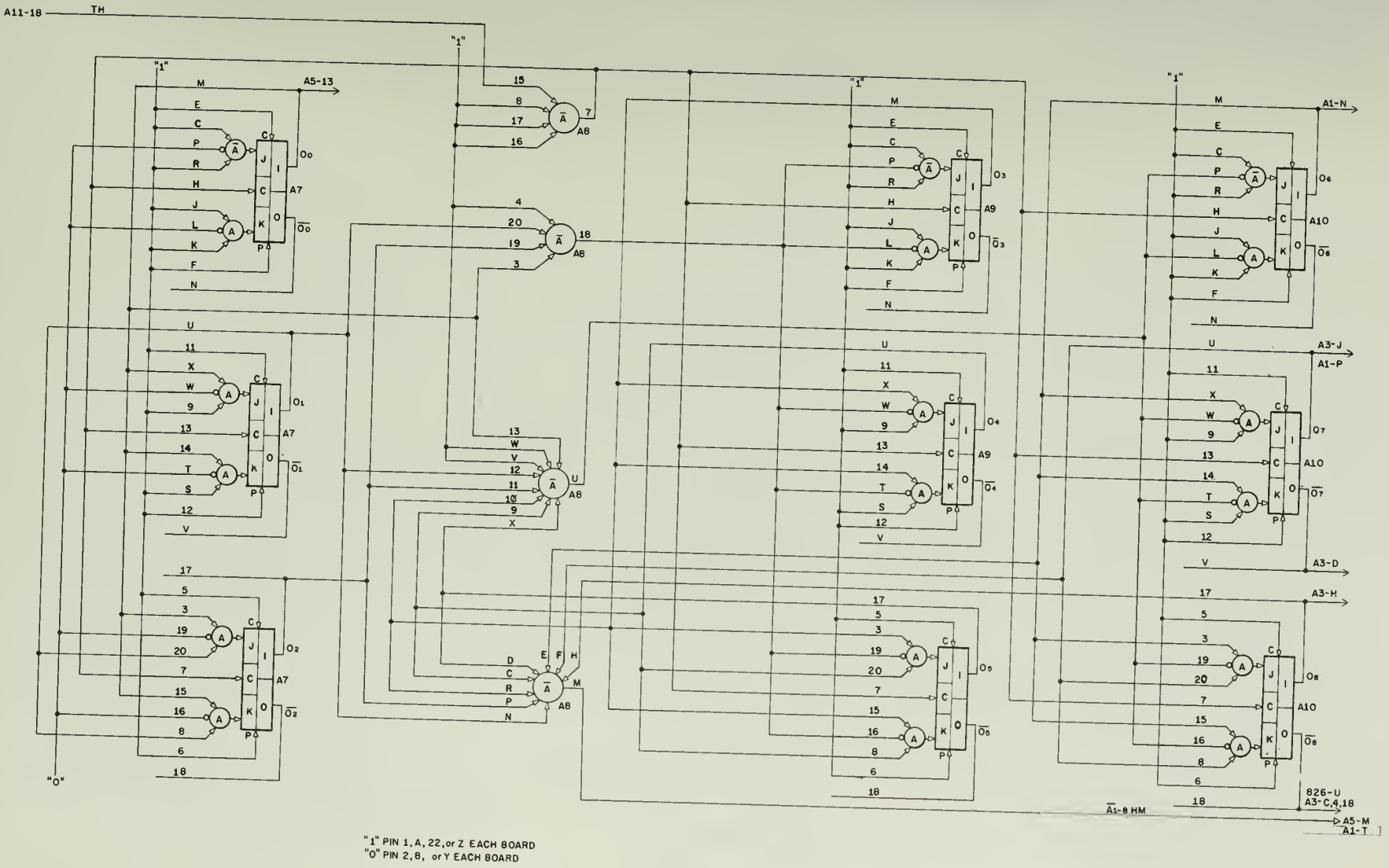


Figure A3.3.2.2 HORIZONTAL MASTER SYNCHRONOUS COUNTER

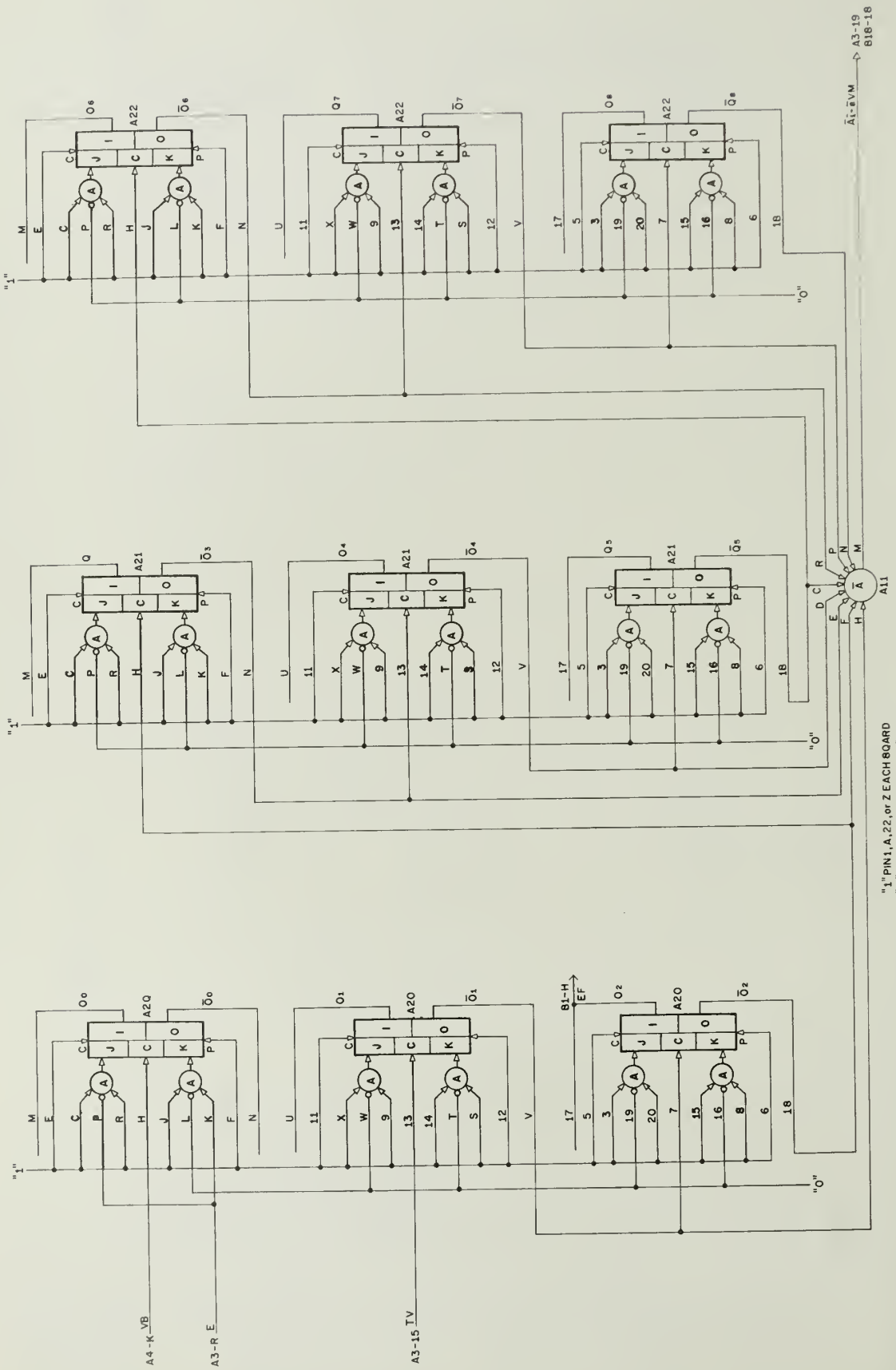


Figure A3.3.2.3 VERTICAL MASTER RIPPLE COUNTER

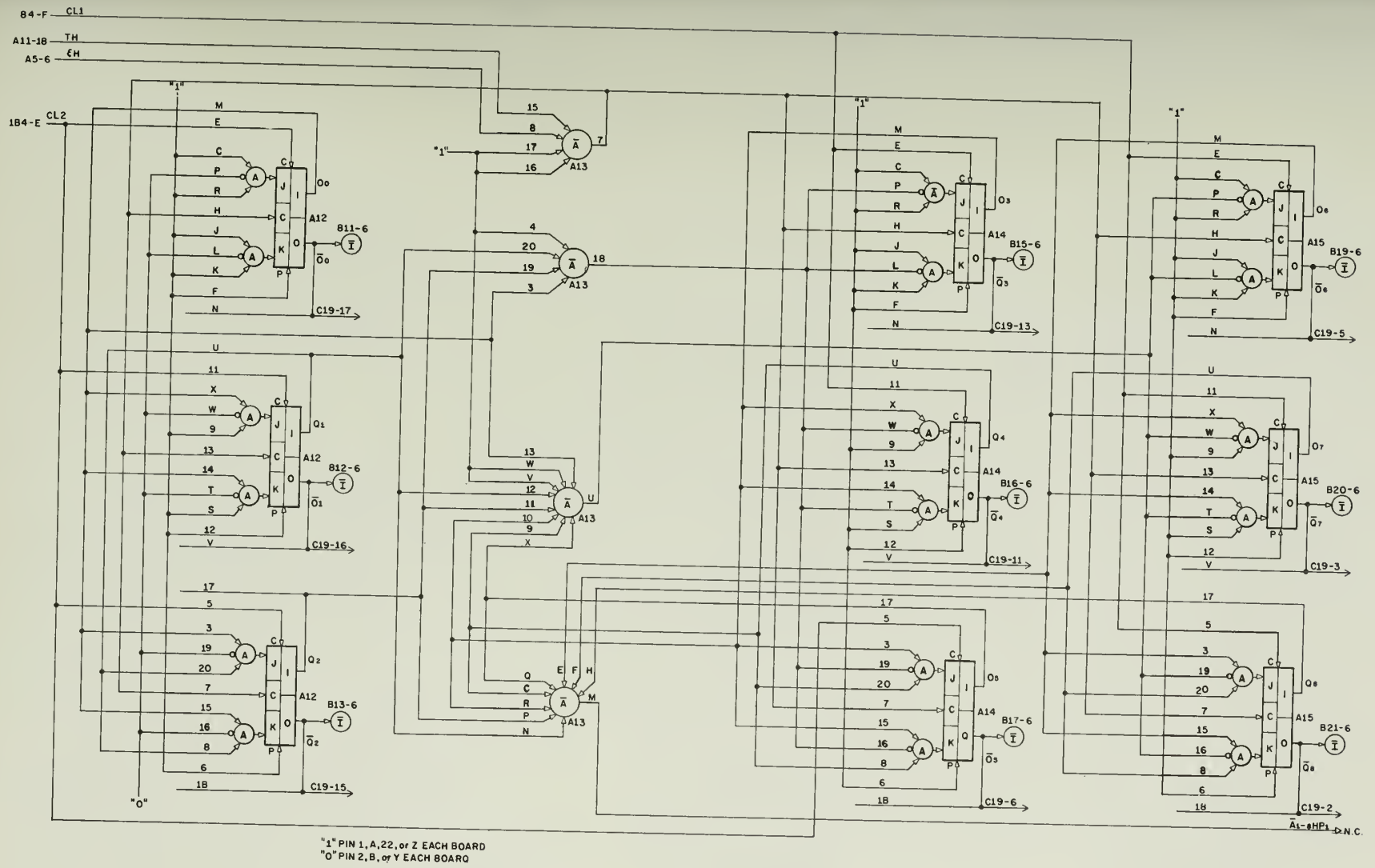


Figure A3.3.2.4 HORIZONTAL POINT 1 SYNCHRONOUS COUNTER

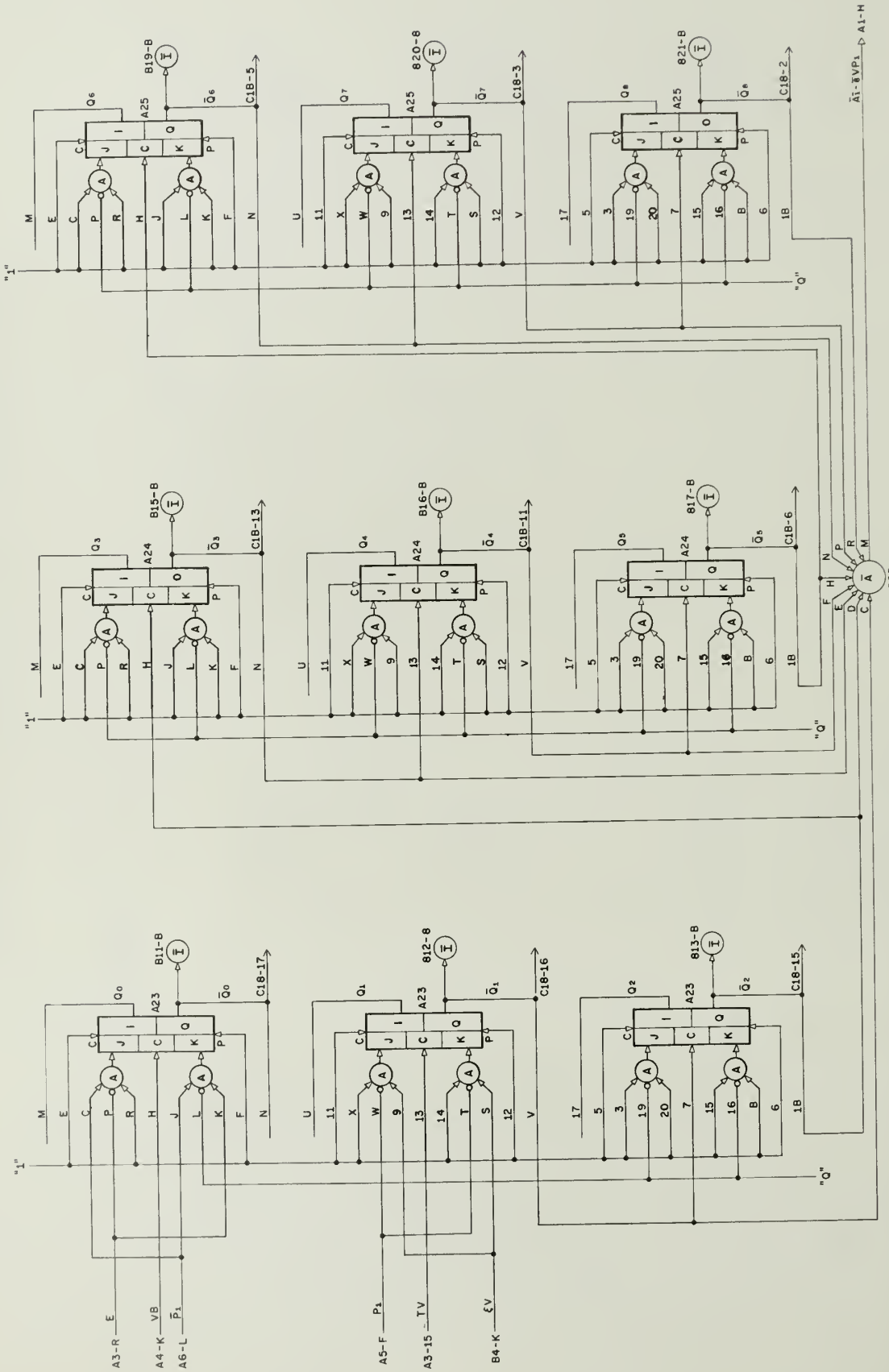


Figure A3.3.2.5 VERTICAL POINT 1 RIPPLE COUNTER

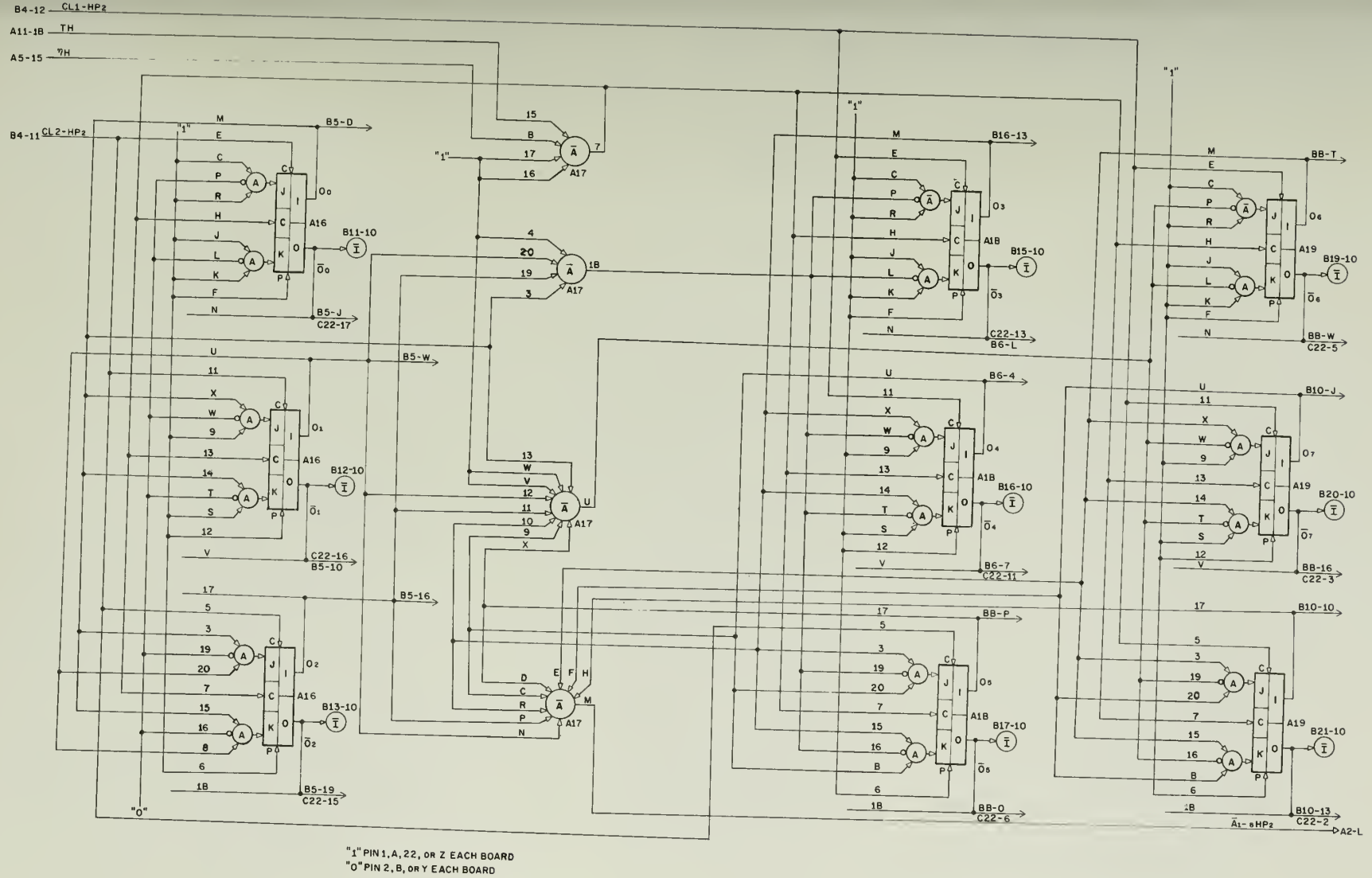


Figure A3.3.2.6 HORIZONTAL POINT 2 SYNCHRONOUS COUNTER

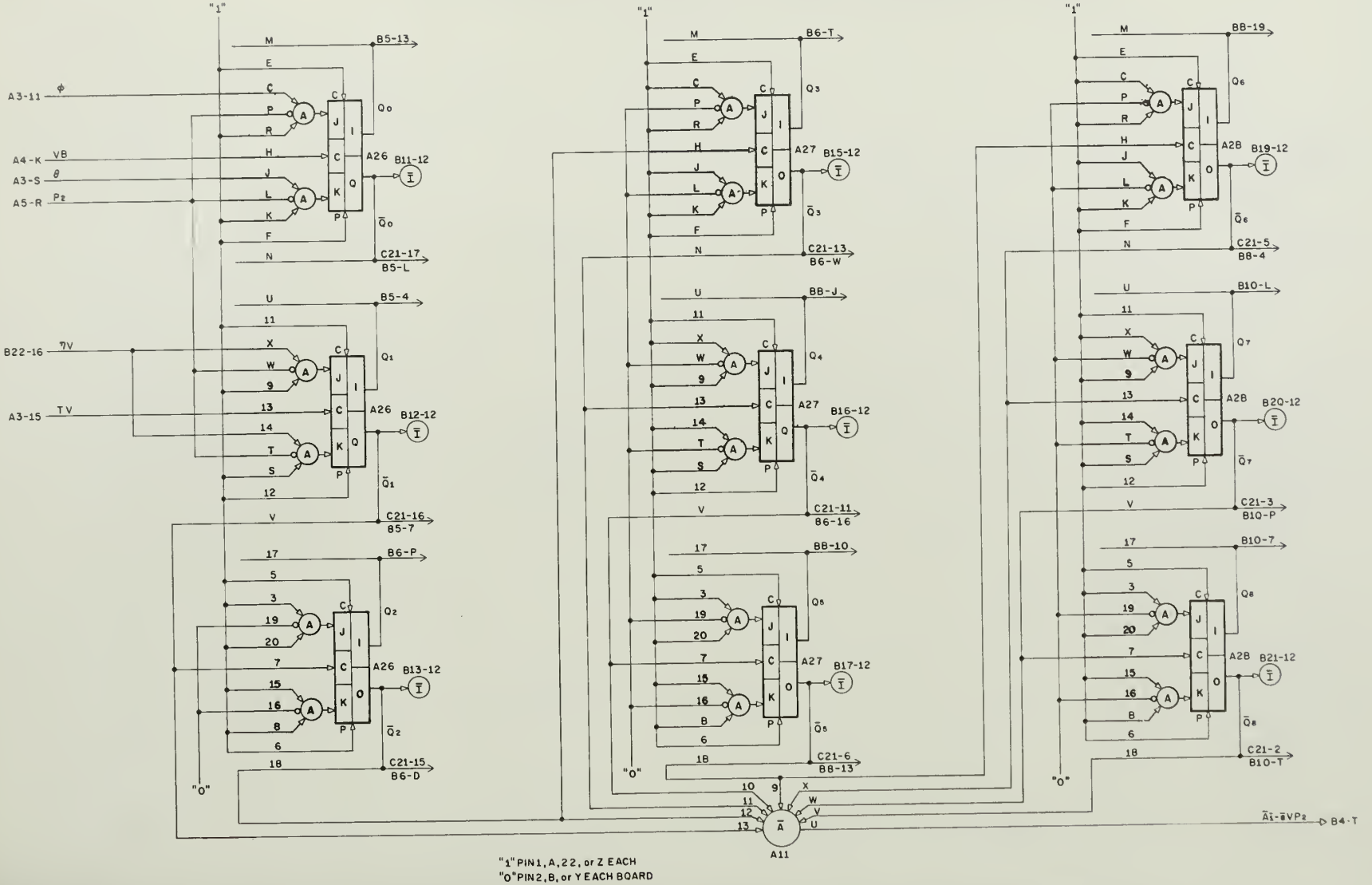


Figure A3.3.2.7 VERTICAL POINT 2 RIPPLE COUNTER

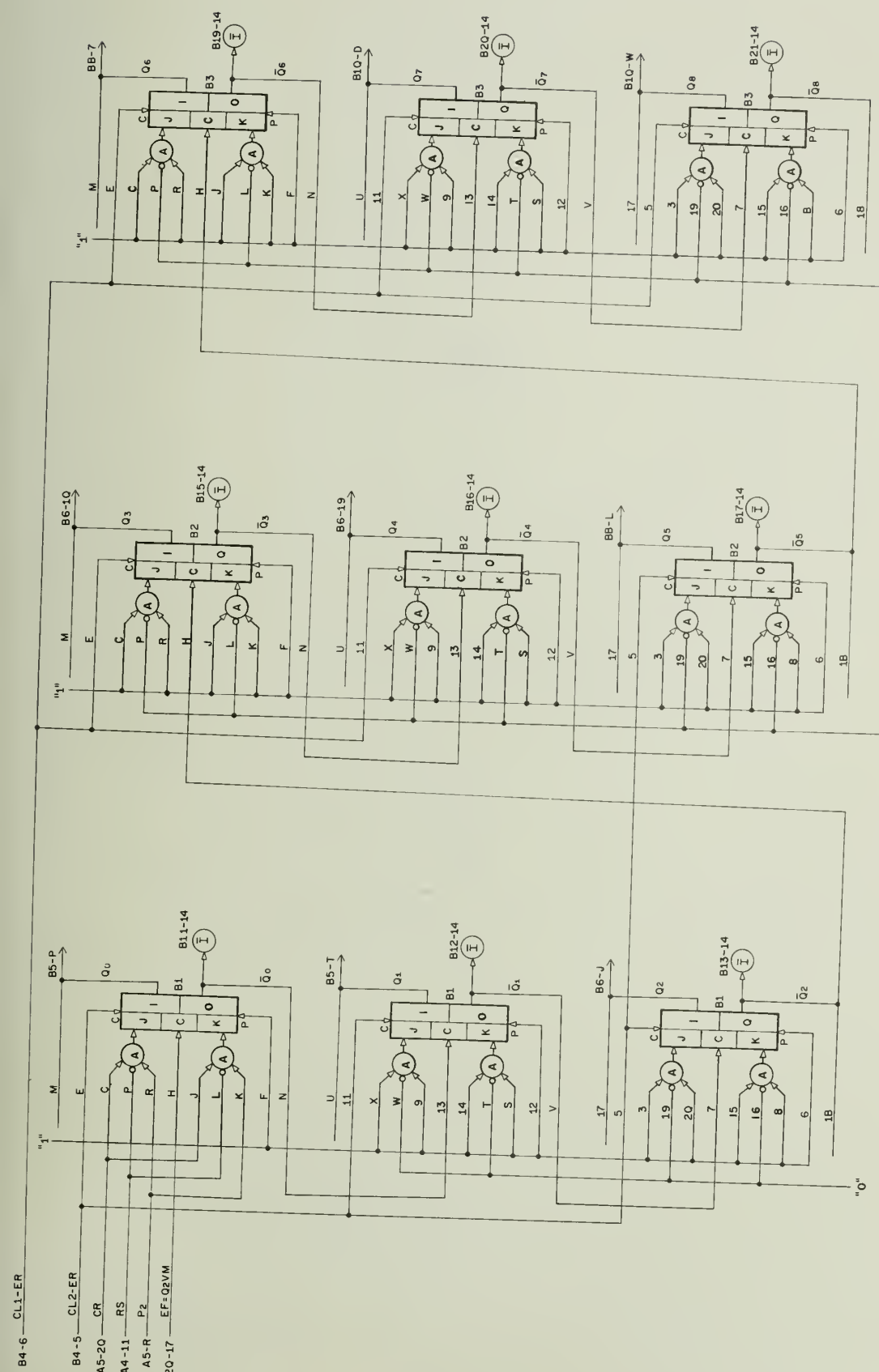


Figure A3.3.2.8 EXPANDING RADIUS RIPPLE COUNTER

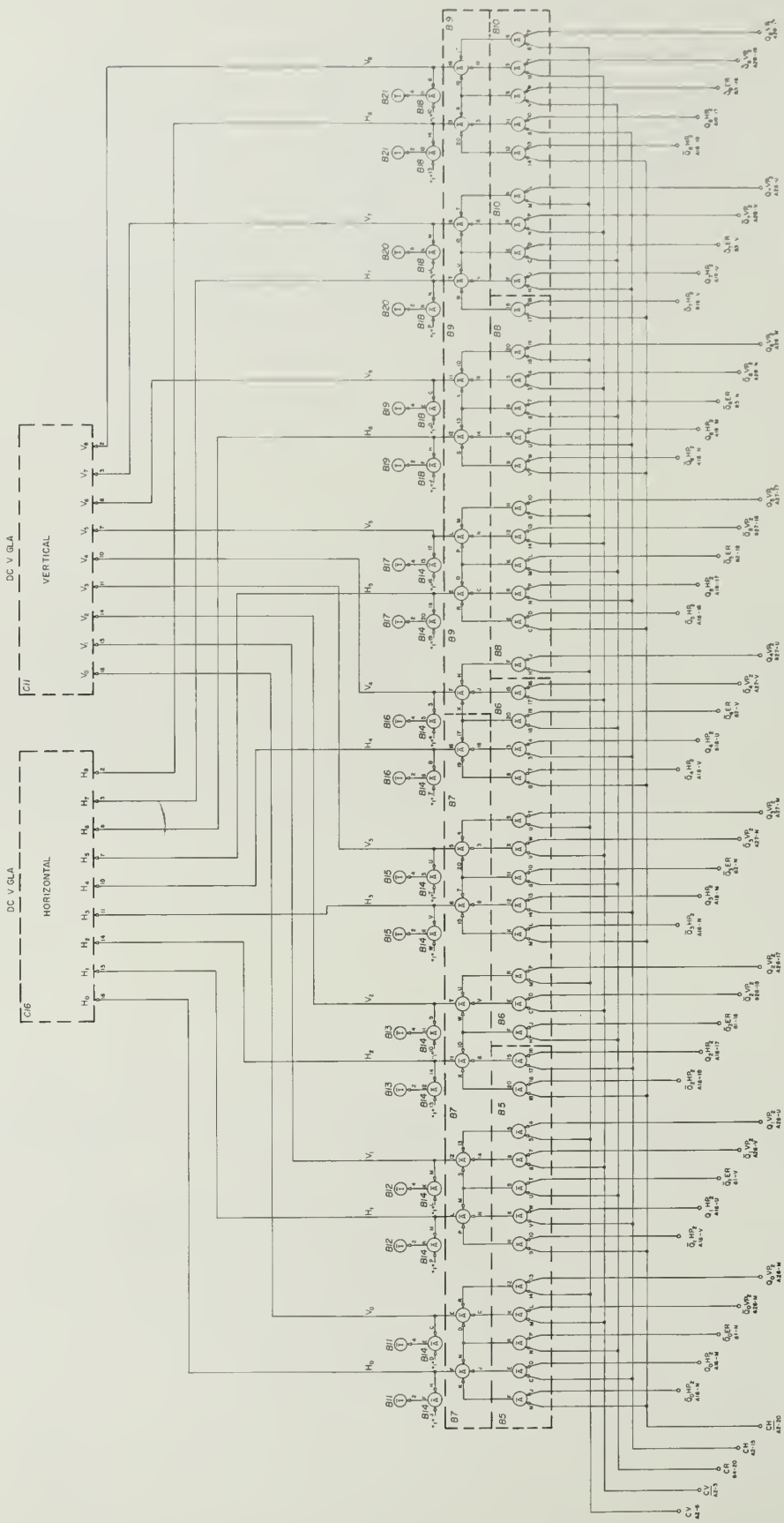


Figure A3.3.2.9 SWITCHING CIRCUIT

A3.3.3 PROCESSOR - Hybrid Section

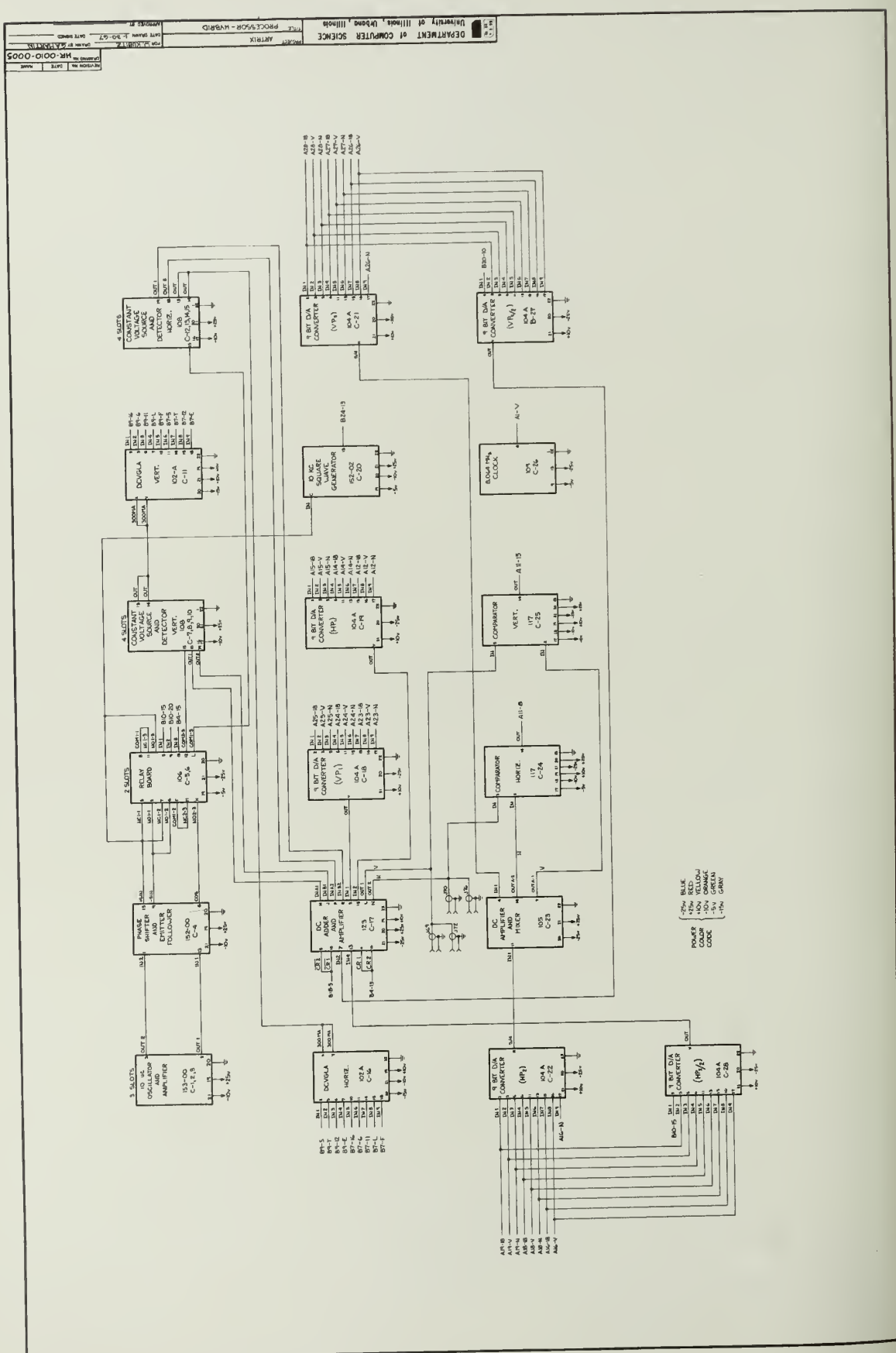
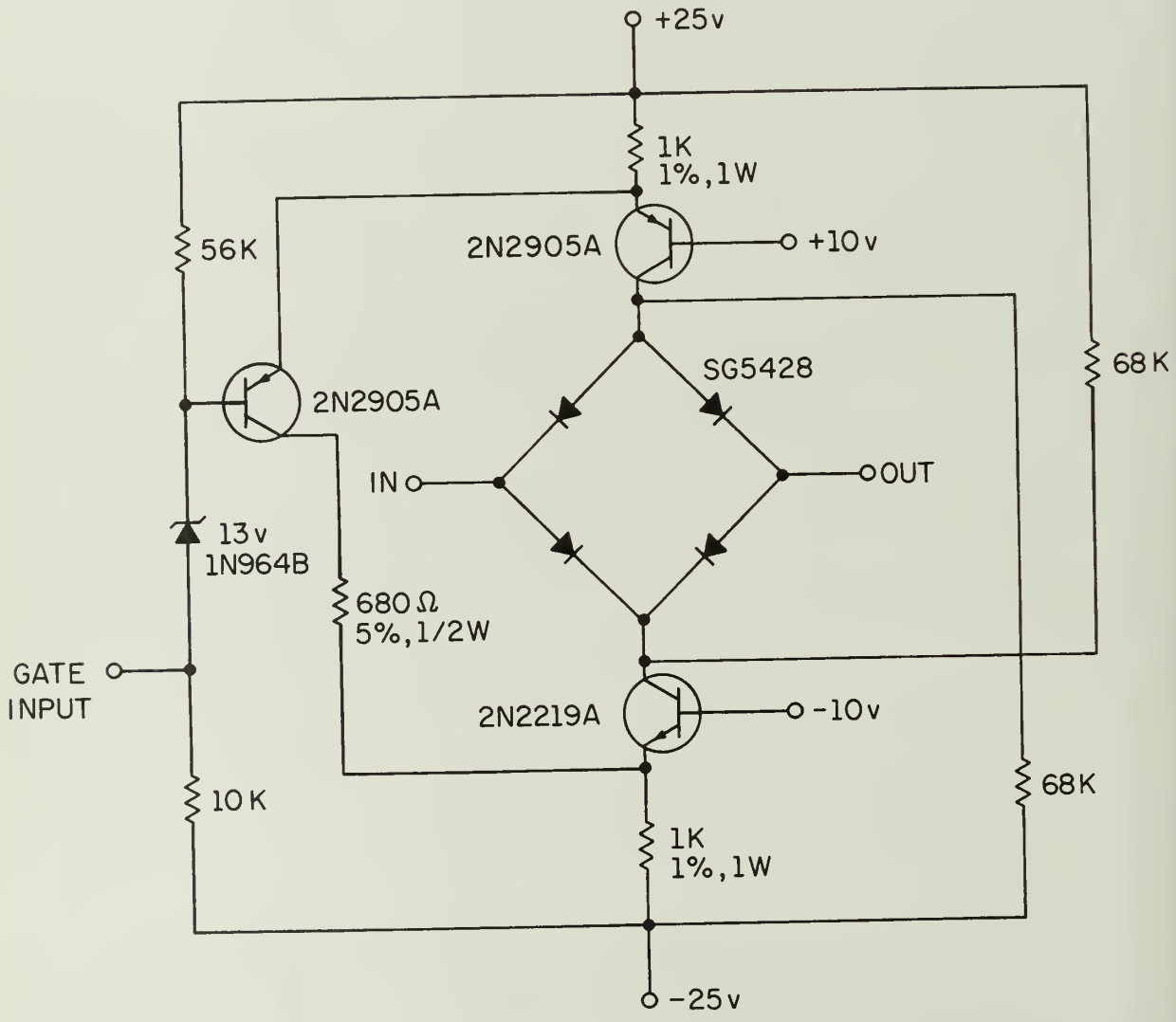


Figure A3.3.3.1 PROCESSOR - Hybrid

A3.4 Circuit Card Schematics

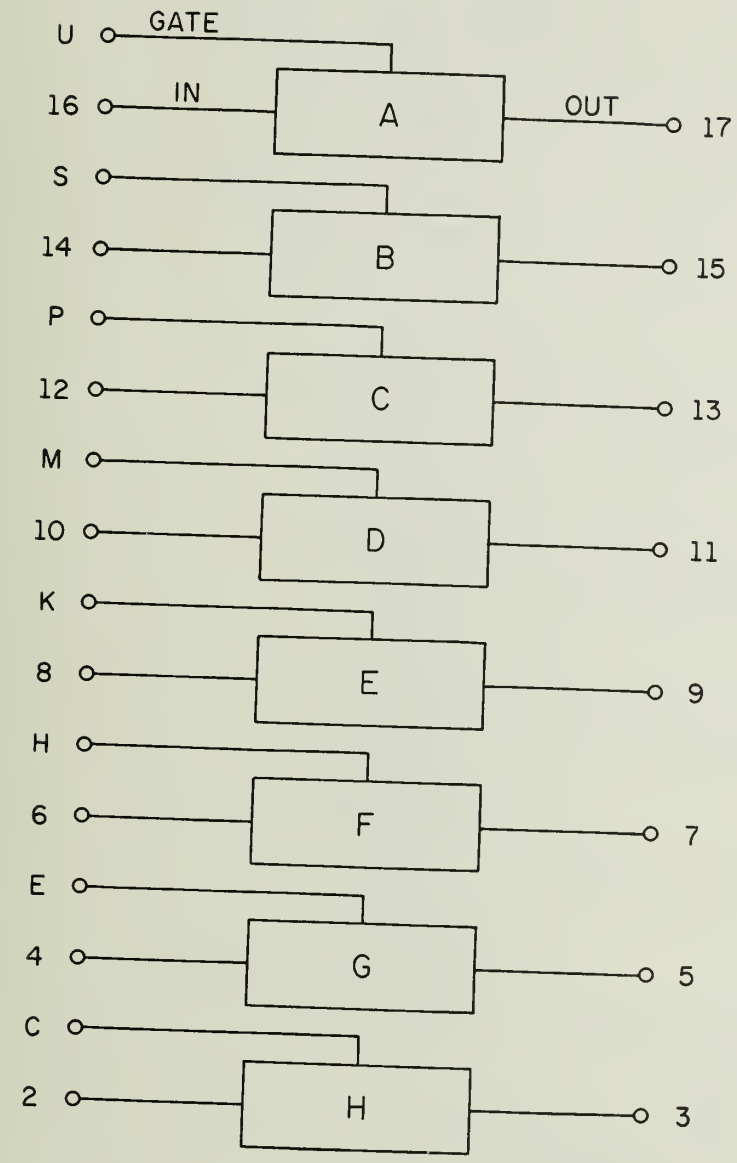
1469-14A
DIAMOND (ANALOG) GATE

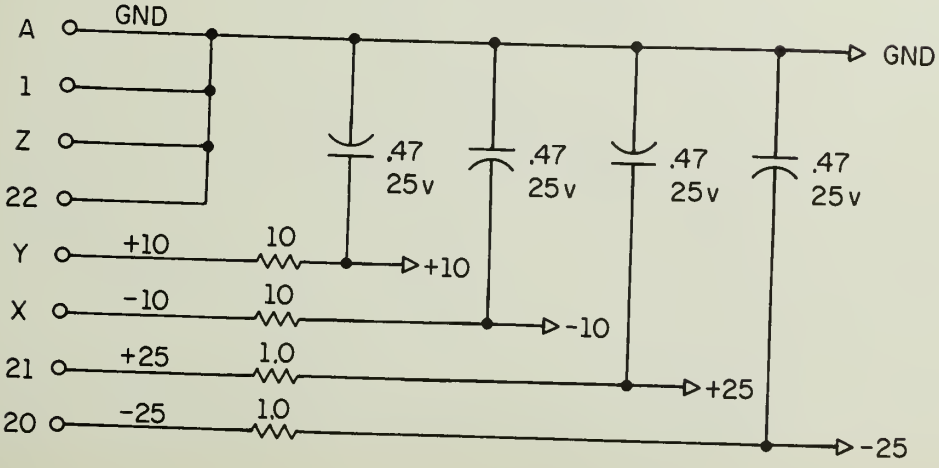


NOTES

1. ALL RESISTORS 5%, 1/4W EXCEPT AS NOTED
2. SEE NEXT PAGE FOR PIN AND VOLTAGE CONNECTIONS

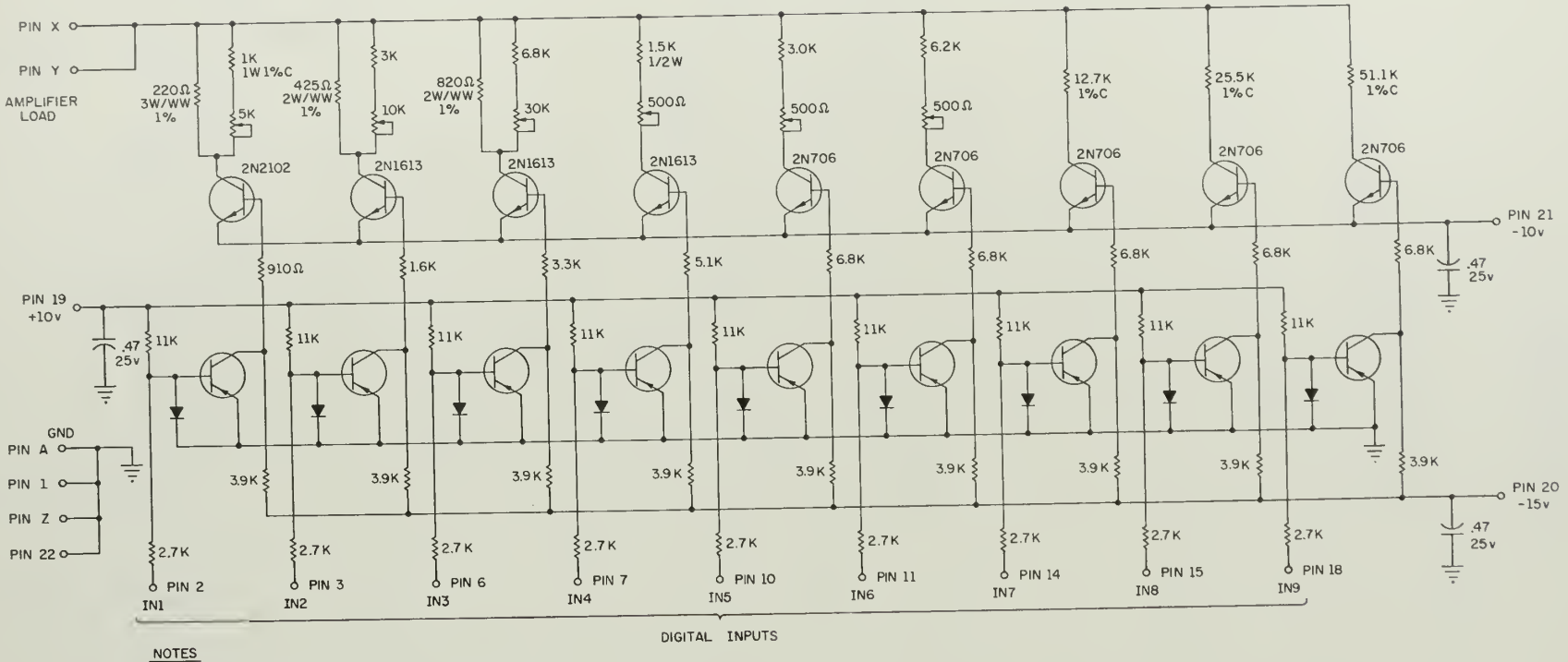
1469 - 14A
DIAMOND (ANALOG) GATE





1469-102B

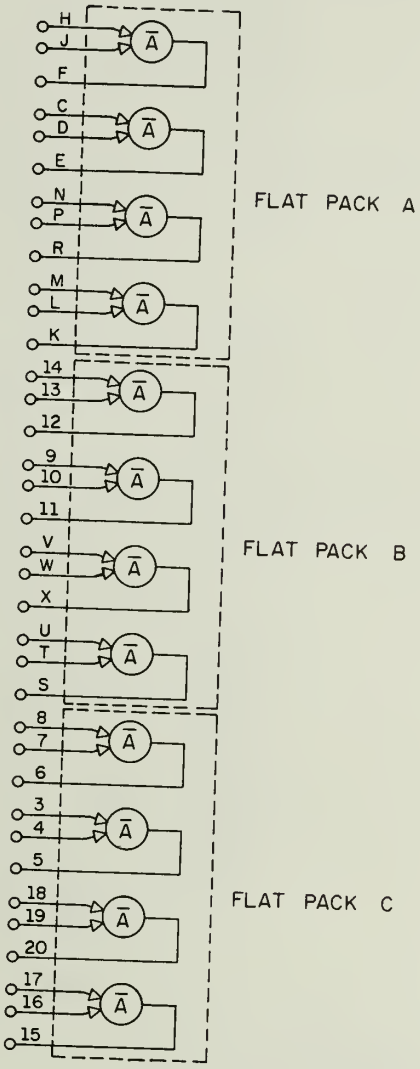
DIGITALLY CONTROLLED, VARIABLE GAIN, LINEAR AMPLIFIER

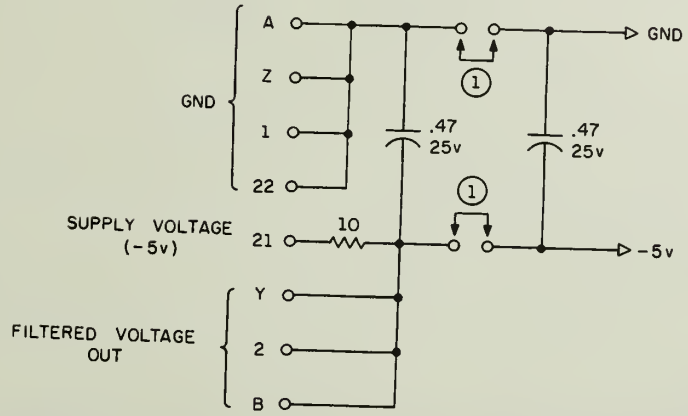


NOTES

1. ALL RESISTORS 1/4 W, 5% C UNLESS SPECIFIED
2. ALL TRANSISTORS 2N1305 UNLESS SPECIFIED
3. ALL DIODES 1N995

1469-103B-00 TWO INPUT NAND INTEGRATED CIRCUITS

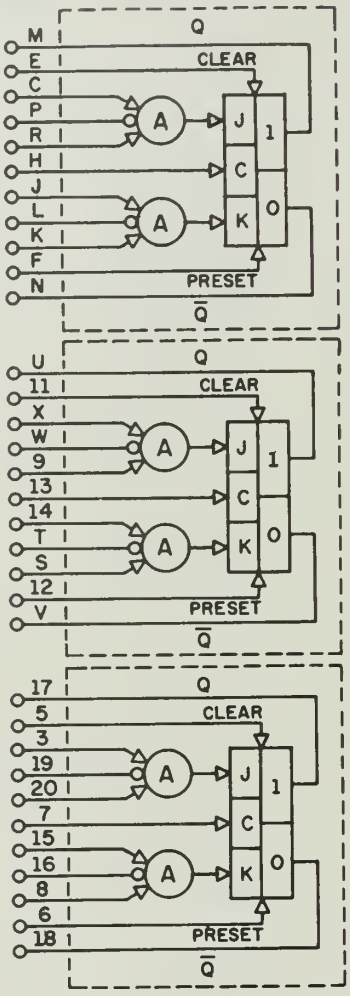


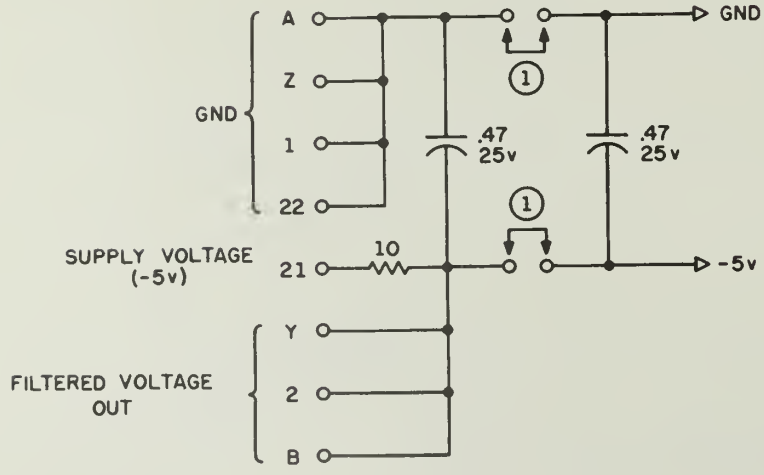


NOTES

(1.) JUMPERS ALLOW POSITIVE OR NEGATIVE OPERATION
2. ALL CIRCUITS TEXAS INSTRUMENTS SN7400

1469-103B-01 J-K FLIP-FLOP INTEGRATED CIRCUIT



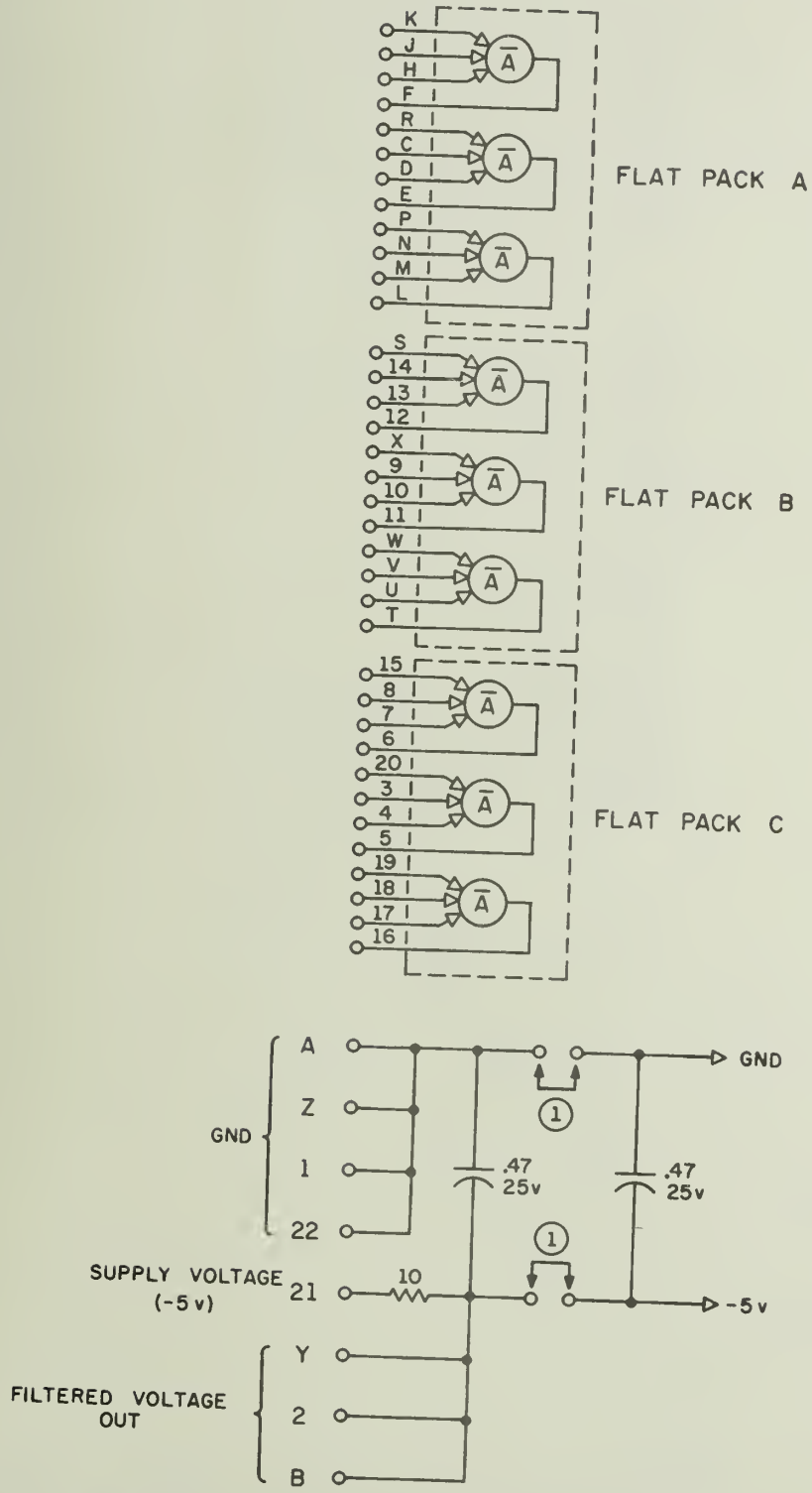


NOTES

(1) JUMPERS ALLOW POSITIVE OR NEGATIVE OPERATION

2. ALL CIRCUITS TEXAS INSTRUMENTS SN7470

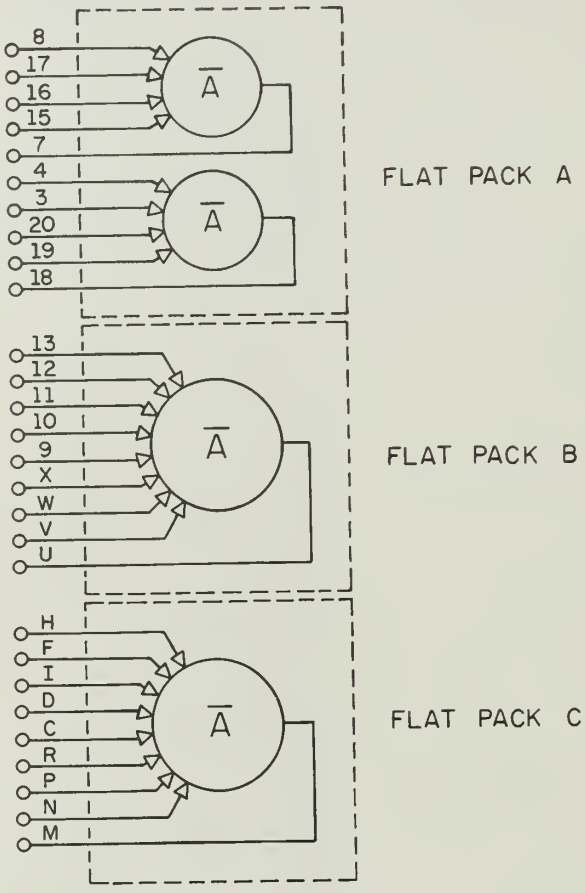
1469-103B-02 3 INPUT NAND INTEGRATED CIRCUIT

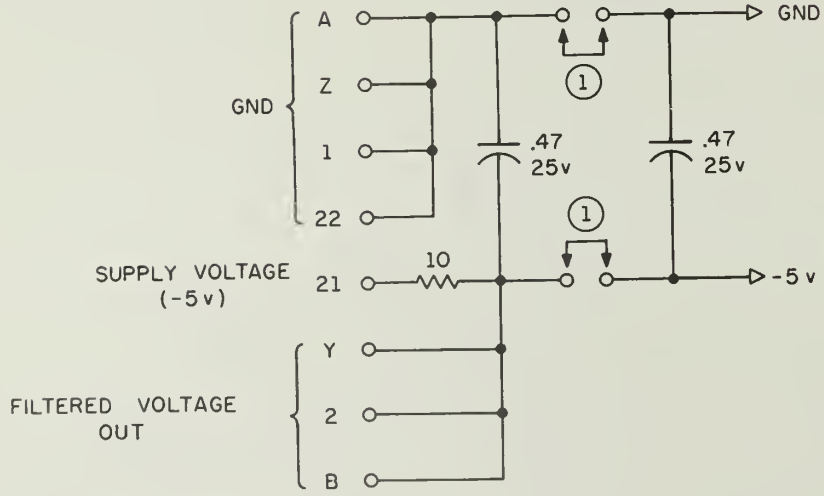


NOTES

(1) JUMPERS ALLOW POSITIVE OR NEGATIVE OPERATION
2. ALL CIRCUITS TEXAS INSTRUMENTS SN7410

1469-103B-03 4 AND 8 INPUT NAND INTEGRATED CIRCUIT



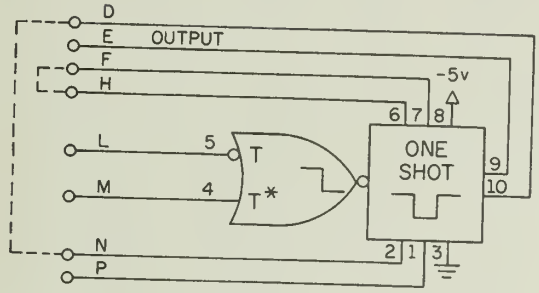


NOTES

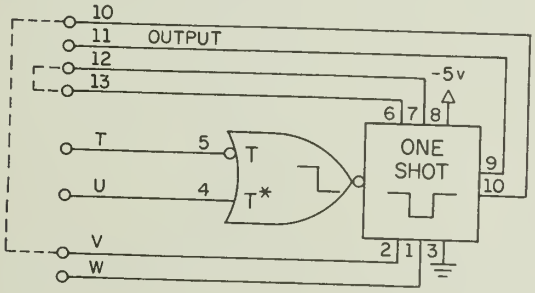
(1.) JUMPERS ALLOW POSITIVE OR NEGATIVE OPERATION

2. ALL CIRCUITS TEXAS INSTRUMENTS SN7440 FOR THE 4 INPUT HANDS AND SN7430 FOR THE 8 INPUT HANDS

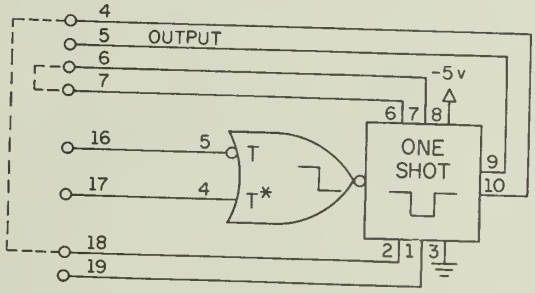
1469-103B-04 MONOSTABLE MULTIVIBRATOR INTEGRATED CIRCUIT



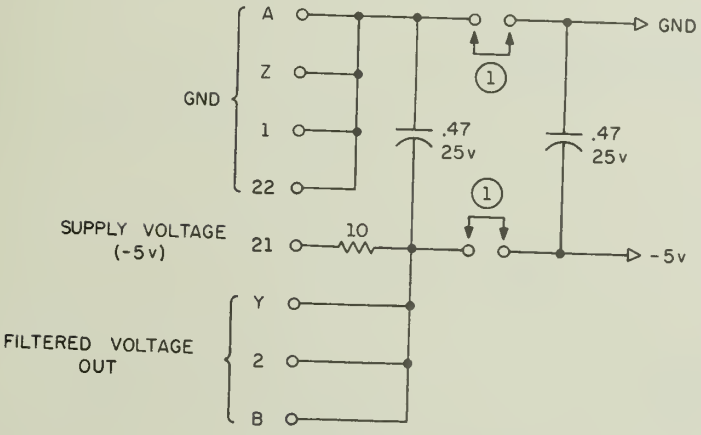
FLAT PACK A



FLAT PACK B



FLAT PACK C

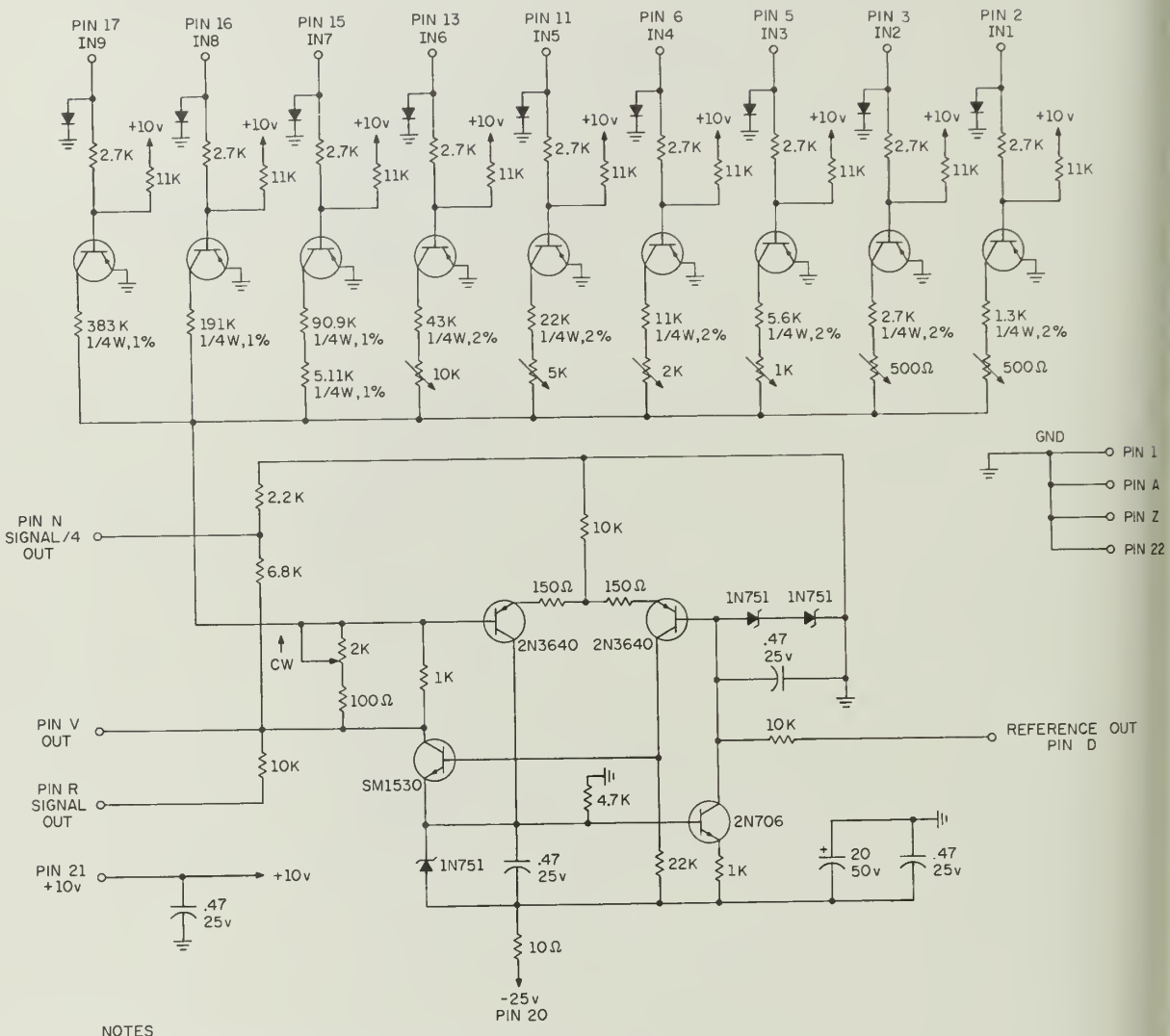


NOTES

(1) JUMPERS ALLOW POSITIVE OR NEGATIVE OPERATION

2. ALL CIRCUITS TEXAS INSTRUMENTS SN7380

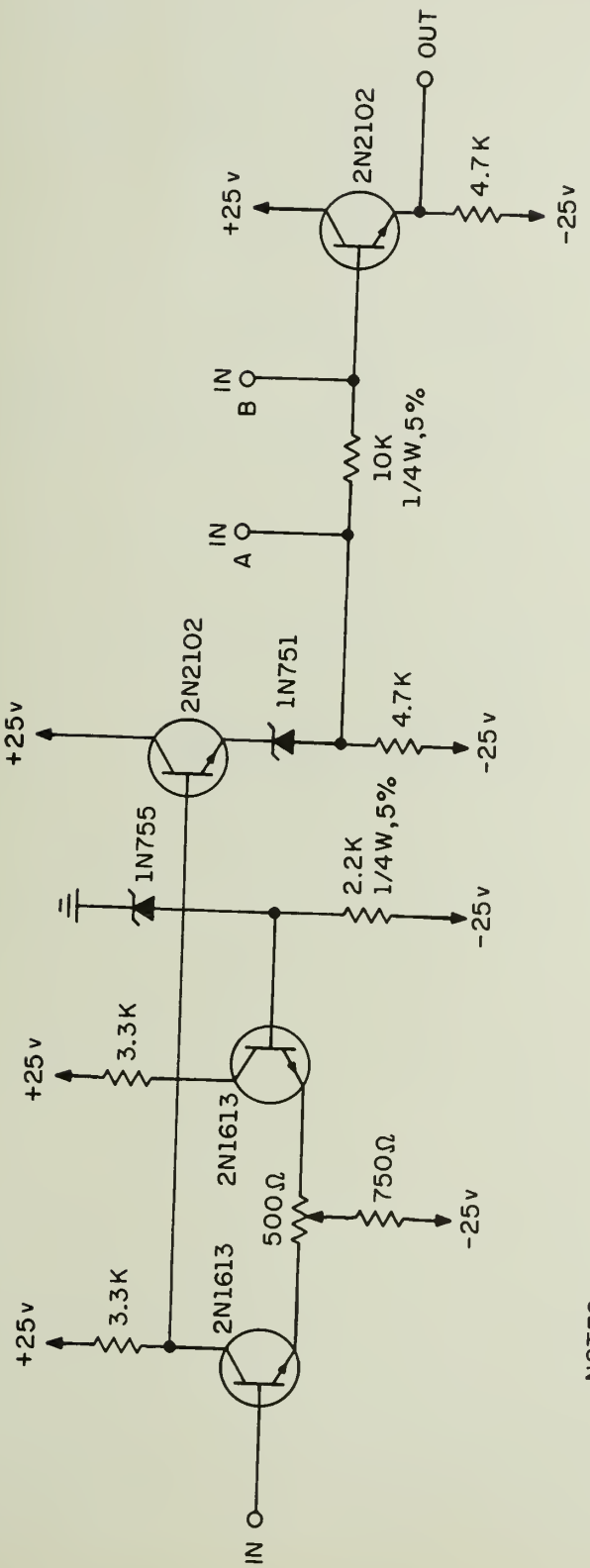
1469-1048 9 BIT D/A CONVERTER



NOTES

1. ALL RESISTORS 1/4 W, 5% UNLESS SPECIFIED
2. ALL TRANSISTORS 2N964 UNLESS SPECIFIED
3. ALL DIODES 1N995 UNLESS SPECIFIED

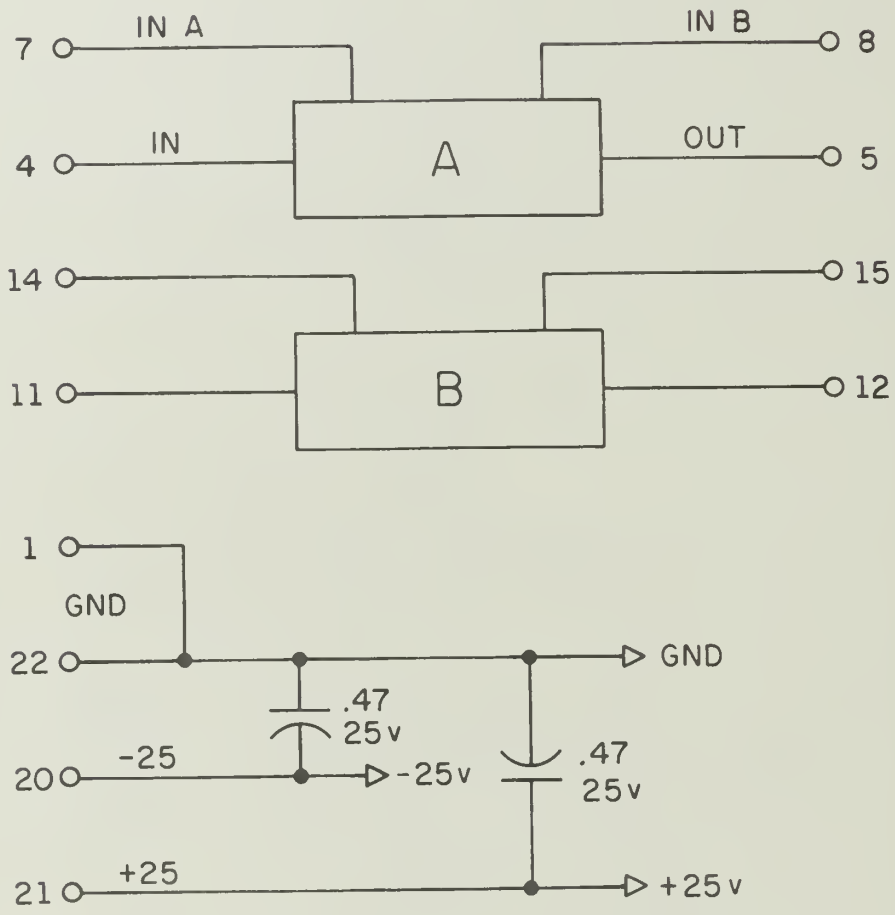
1469-105A DC AMPLIFIER AND MIXER



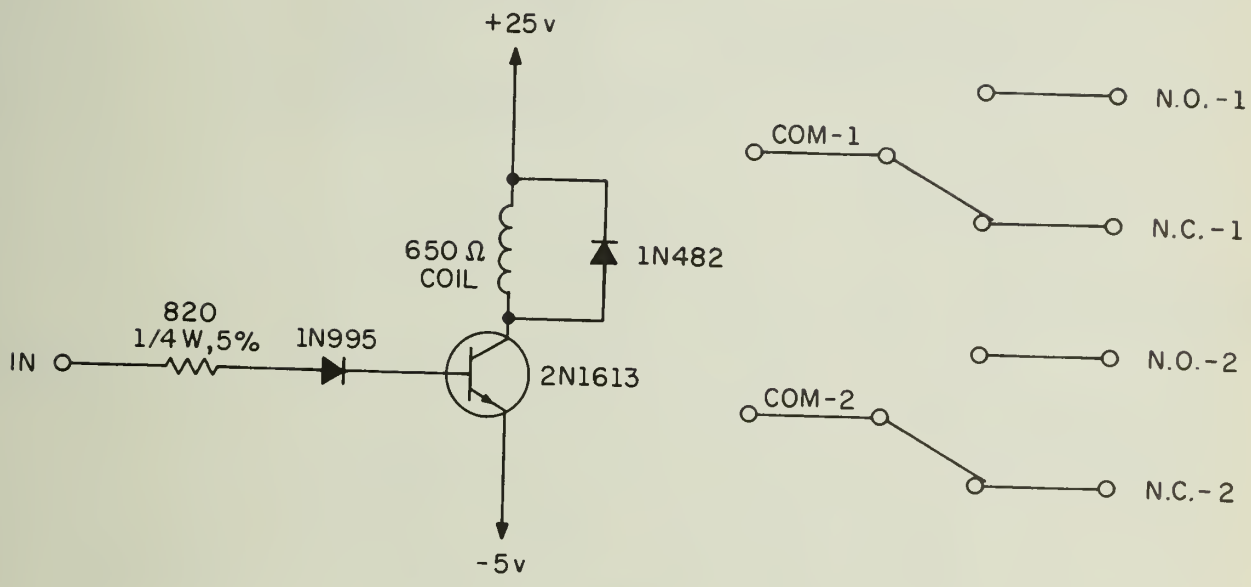
NOTES

1. ALL RESISTORS 1/2 W, 5% UNLESS SPECIFIED.
2. THERE ARE 2 CIRCUITS PER CARD. SEE NEXT PAGE FOR PIN CONNECTIONS.

1469-105A DC AMPLIFIER AND MIXER



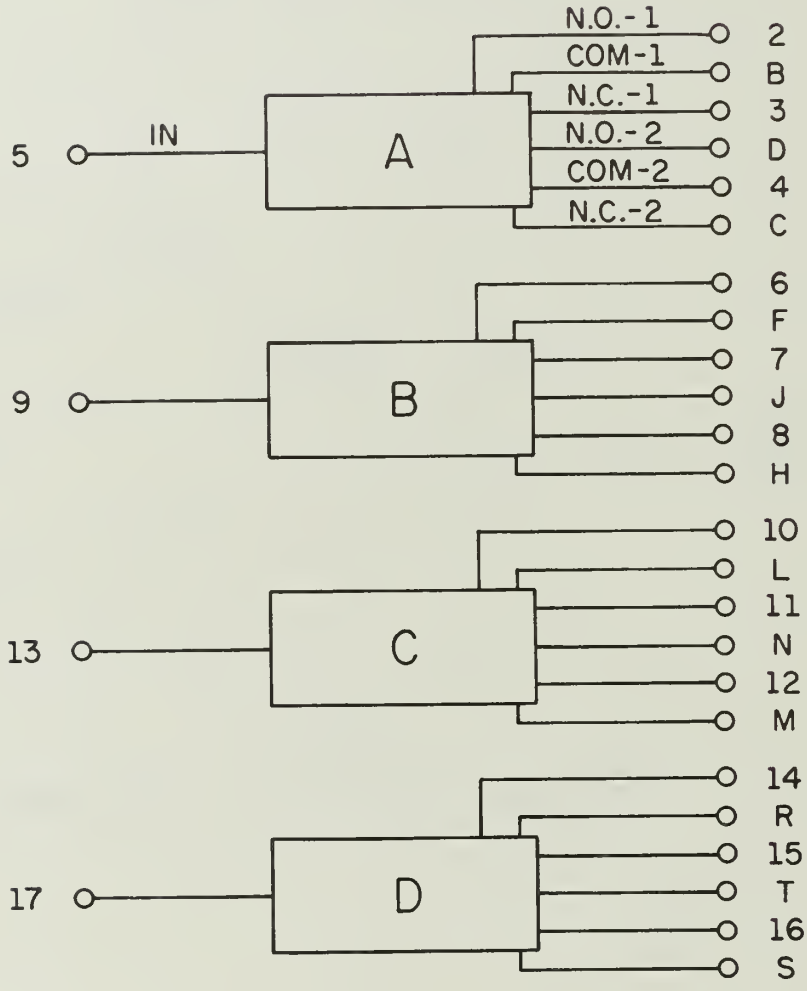
1469-106 DPDT RELAY

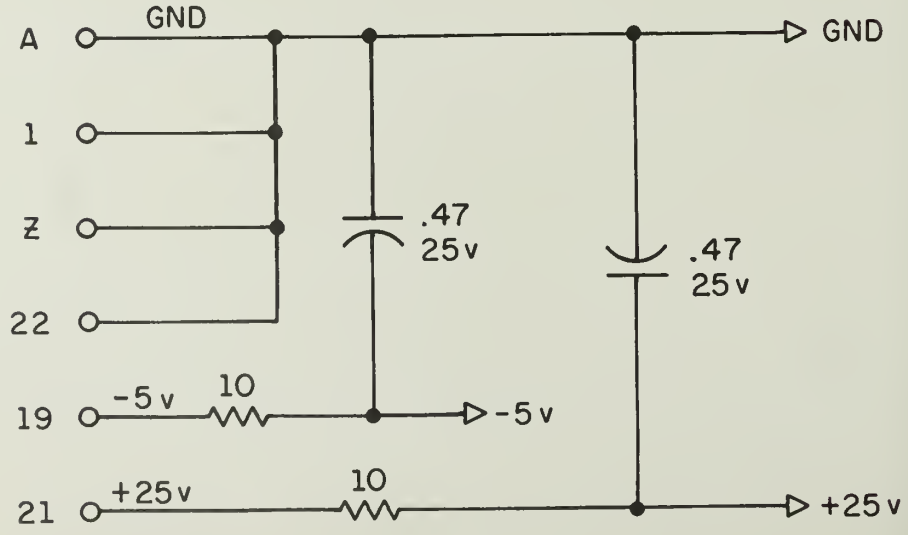


NOTES

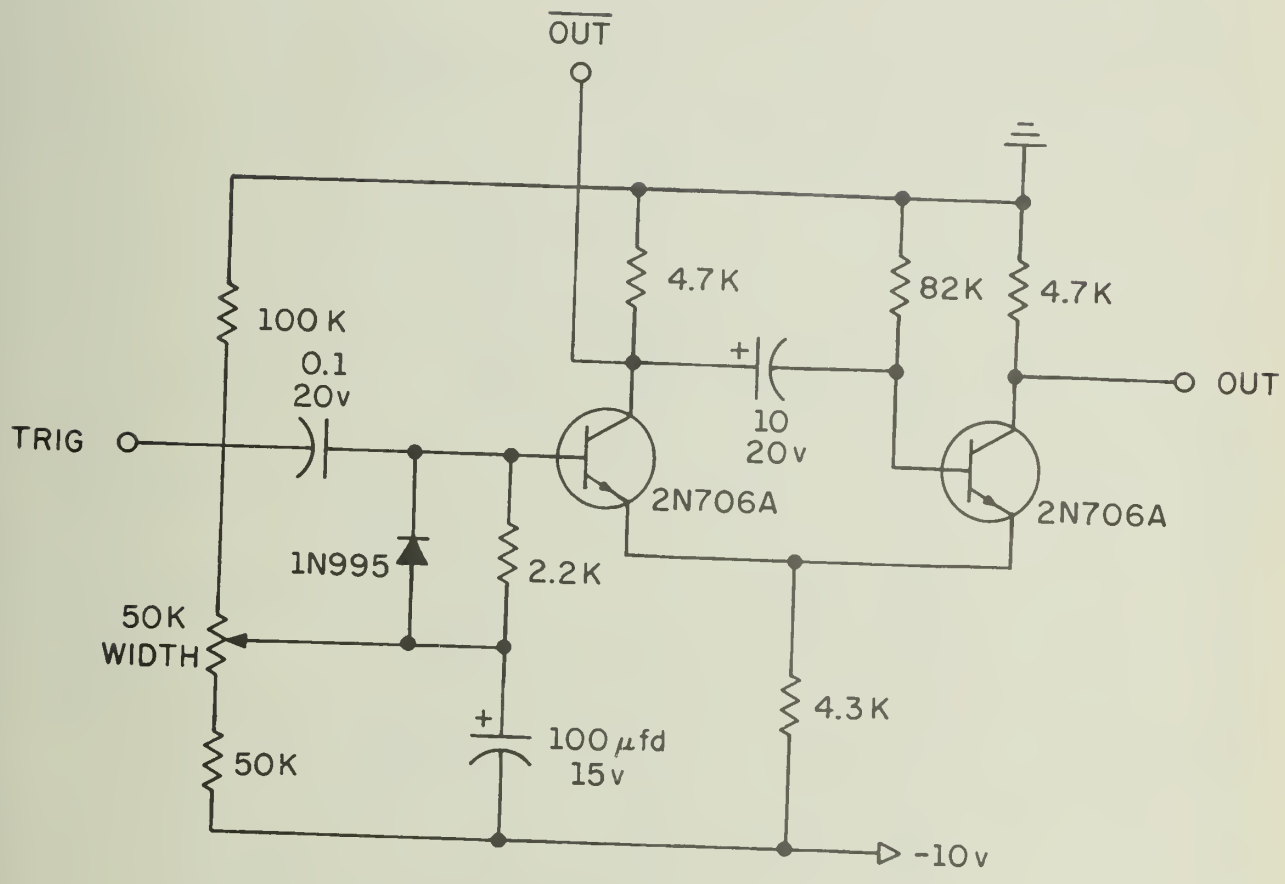
1. SEE NEXT PAGE FOR PIN CONNECTIONS.

1469-106 DPDT RELAY





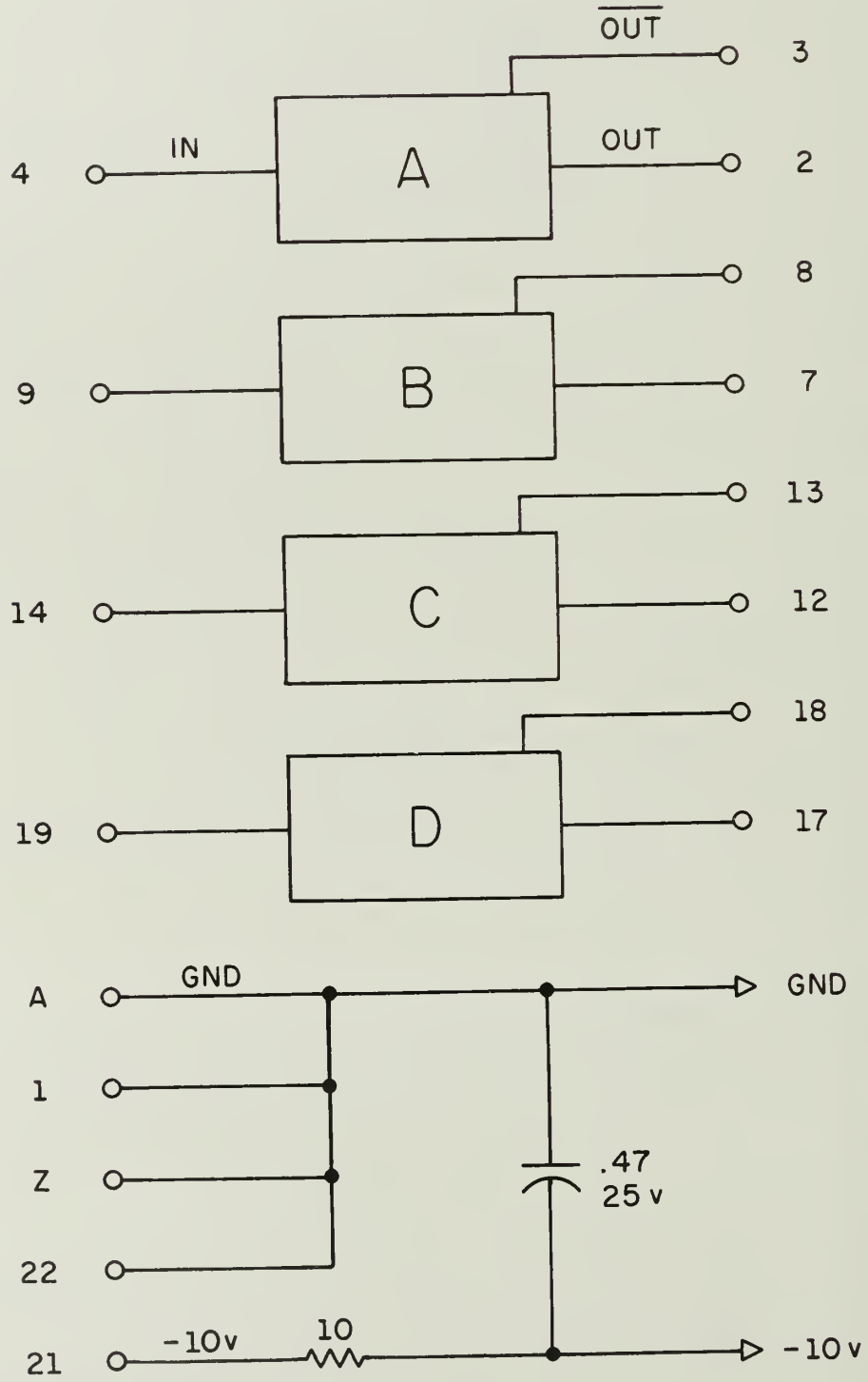
1469-107 10-500 ms DELAY MULTIVIBRATOR



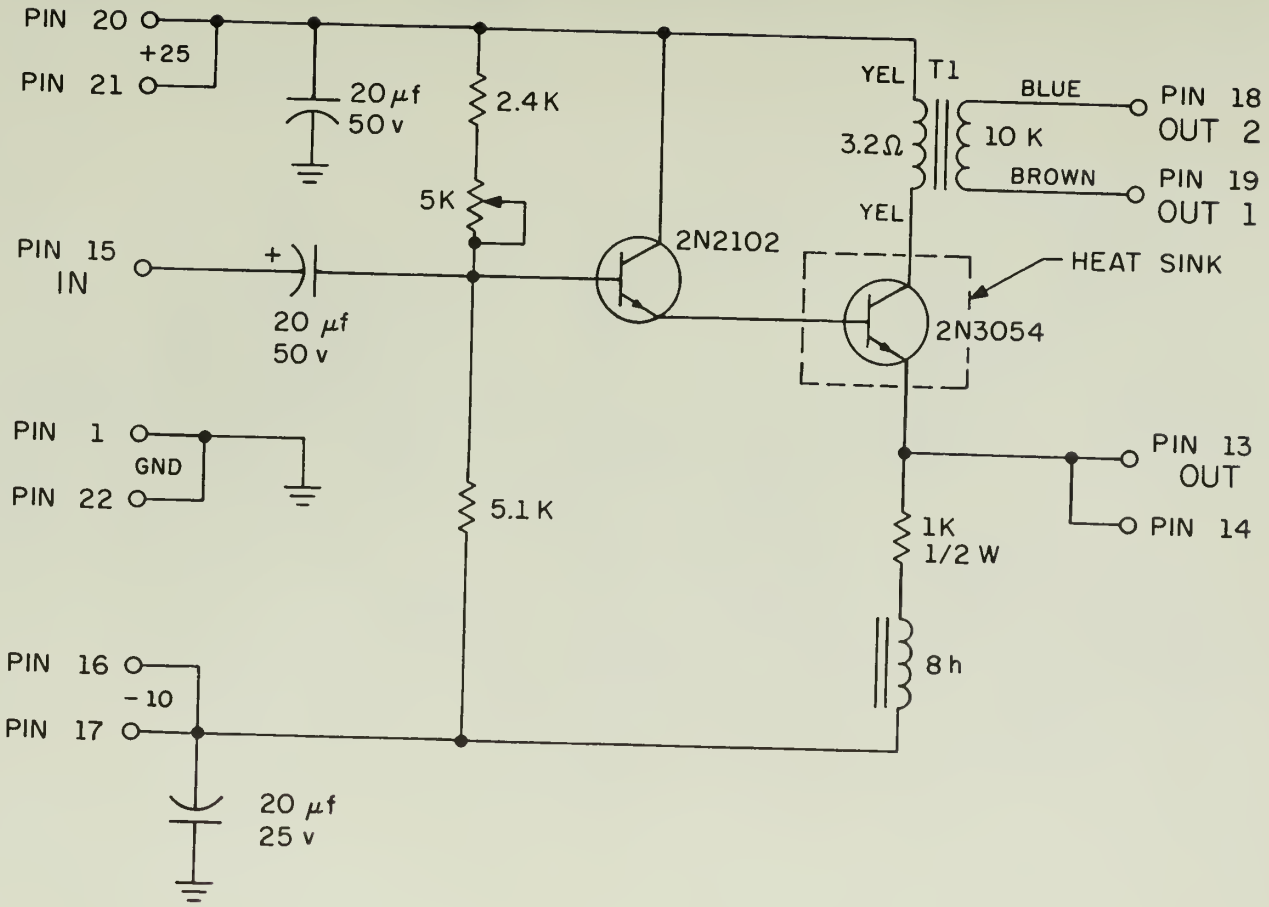
NOTES

1. ALL RESISTORS 1/4 W, 5% UNLESS SPECIFIED.
2. SEE NEXT PAGE FOR PIN CONNECTIONS.

1469-107 10-500 ms DELAY MULTIVIBRATOR



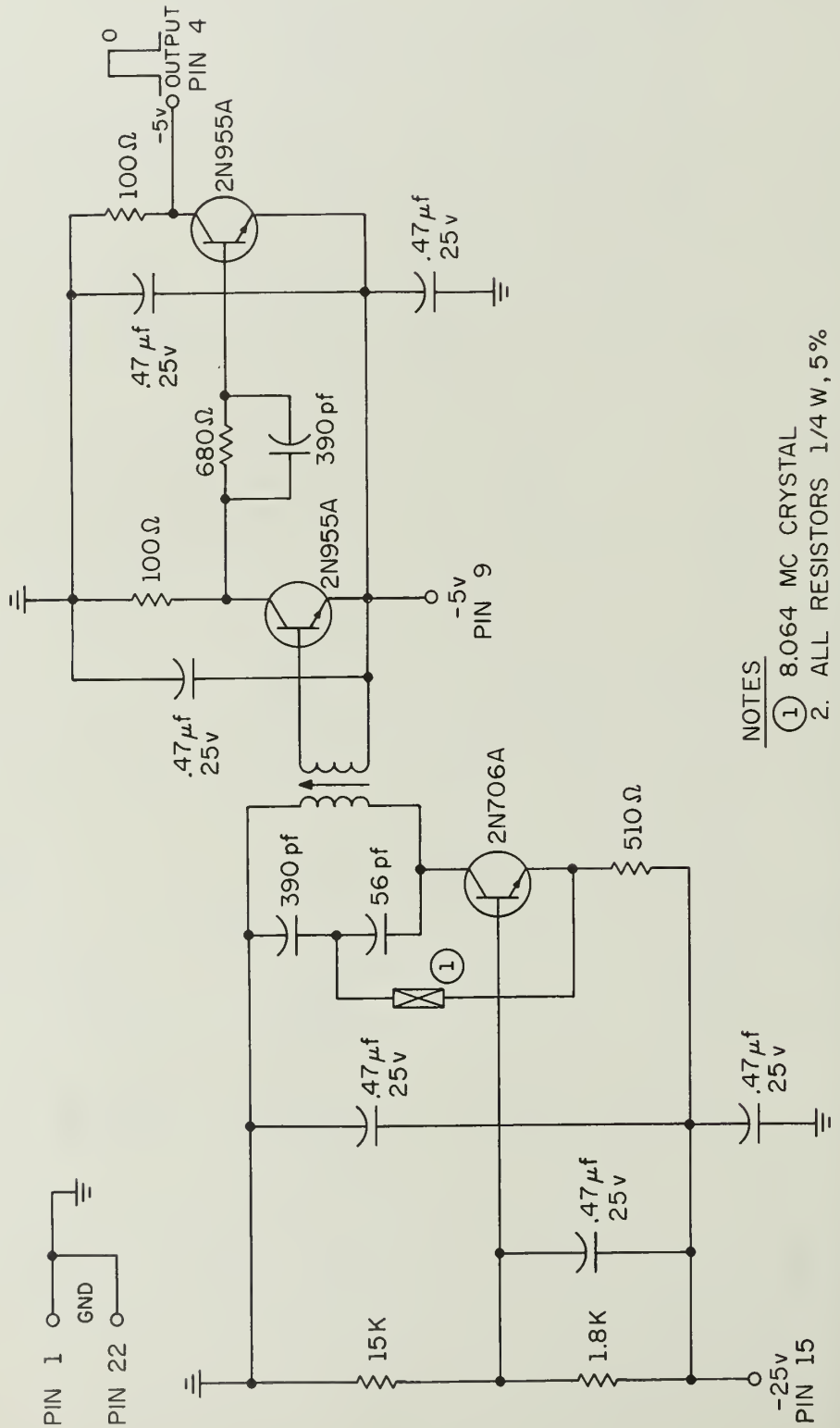
1469-108 CONSTANT VOLTAGE SOURCE AND DETECTOR FOR DCVGLA



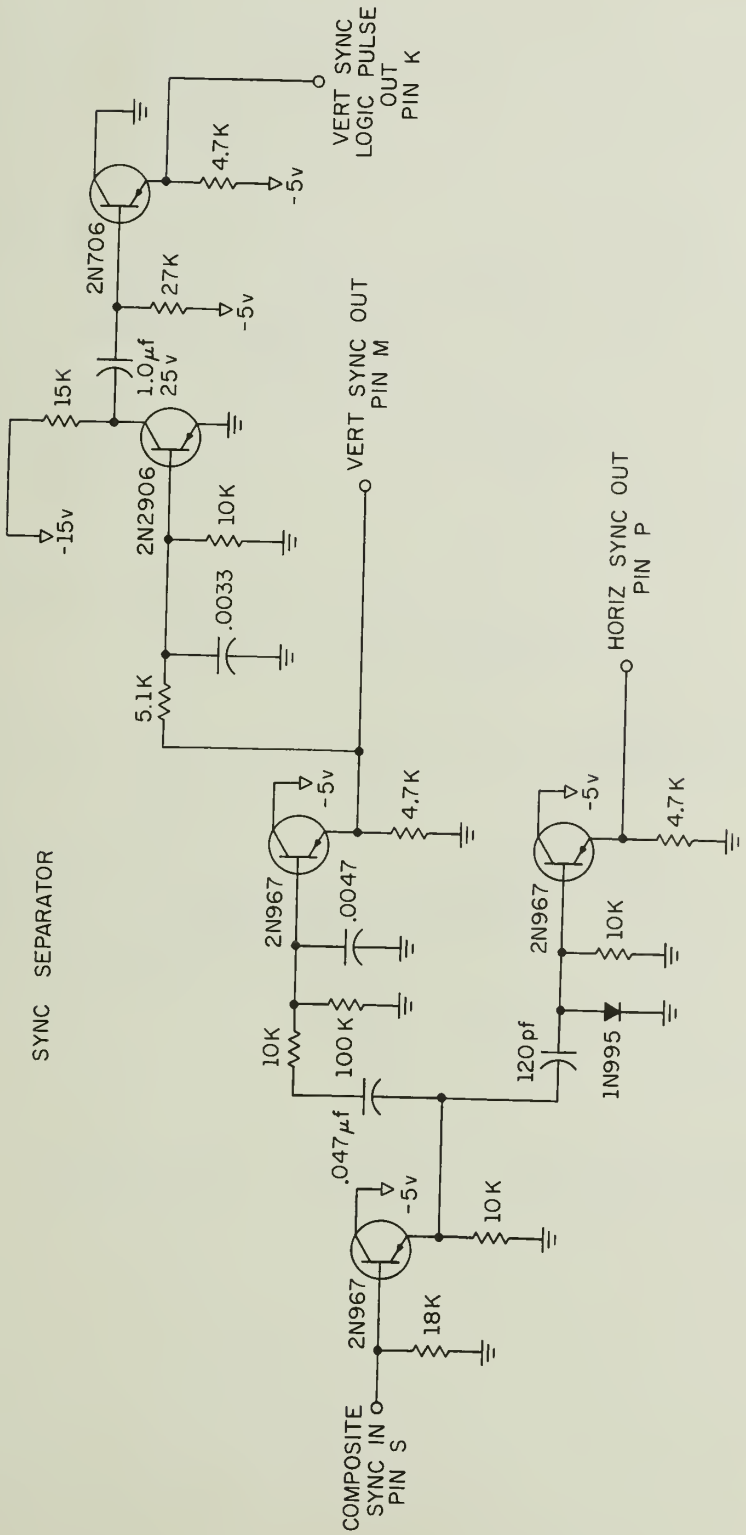
NOTES

1. ALL RESISTORS 1/4 W, 5% UNLESS SPECIFIED.

1469-109 8.064 MC CLOCK

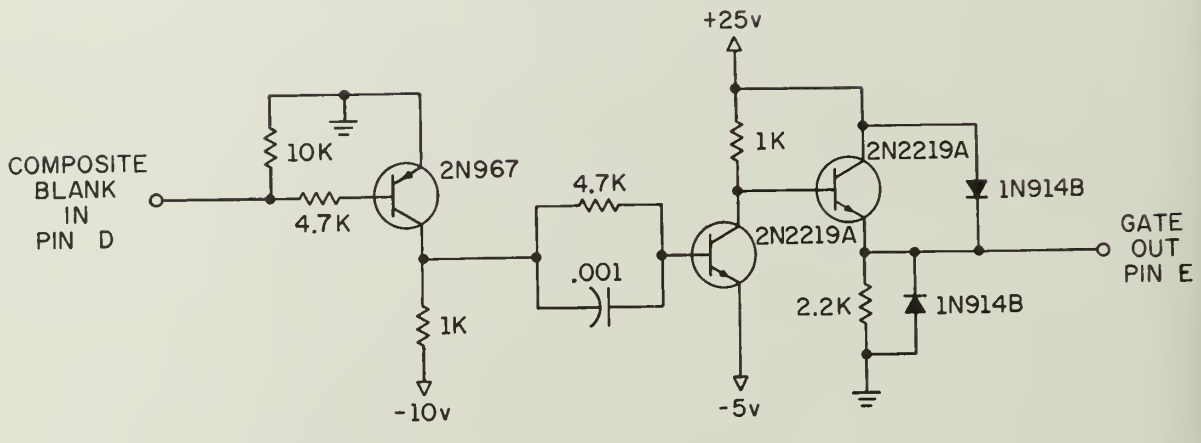


1469-110 SYNC SEPARATOR, GATE DRIVER, VERT BLANKING LOGIC DRIVER

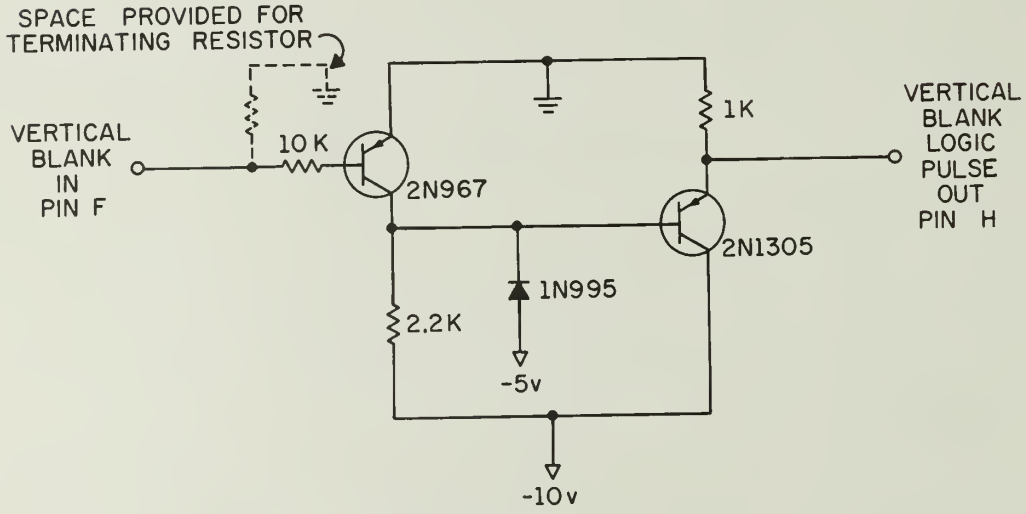


1469-110 SYNC SEPARATOR, GATE DRIVER, VERT. BLANKING LOGIC DRIVER

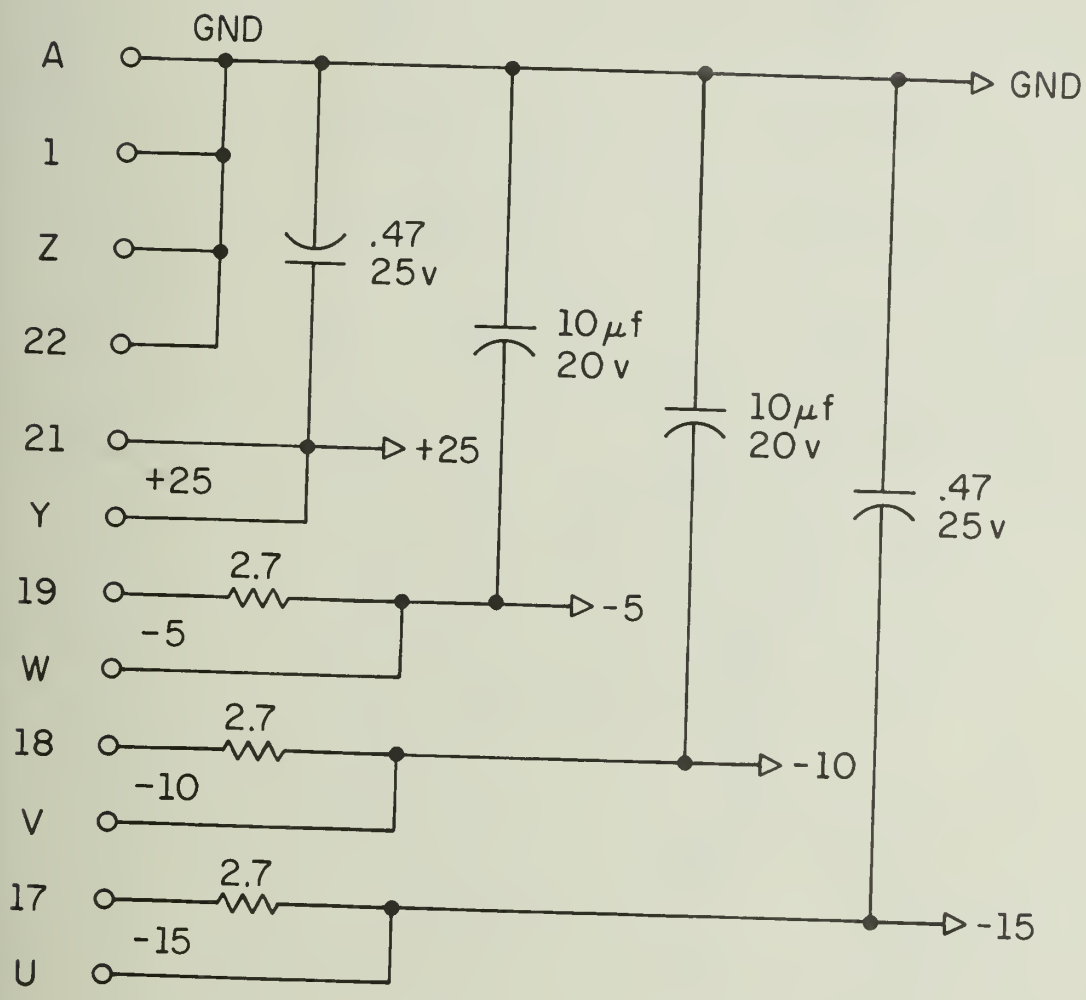
GATE DRIVER



VERT. BLANKING LOGIC DRIVER



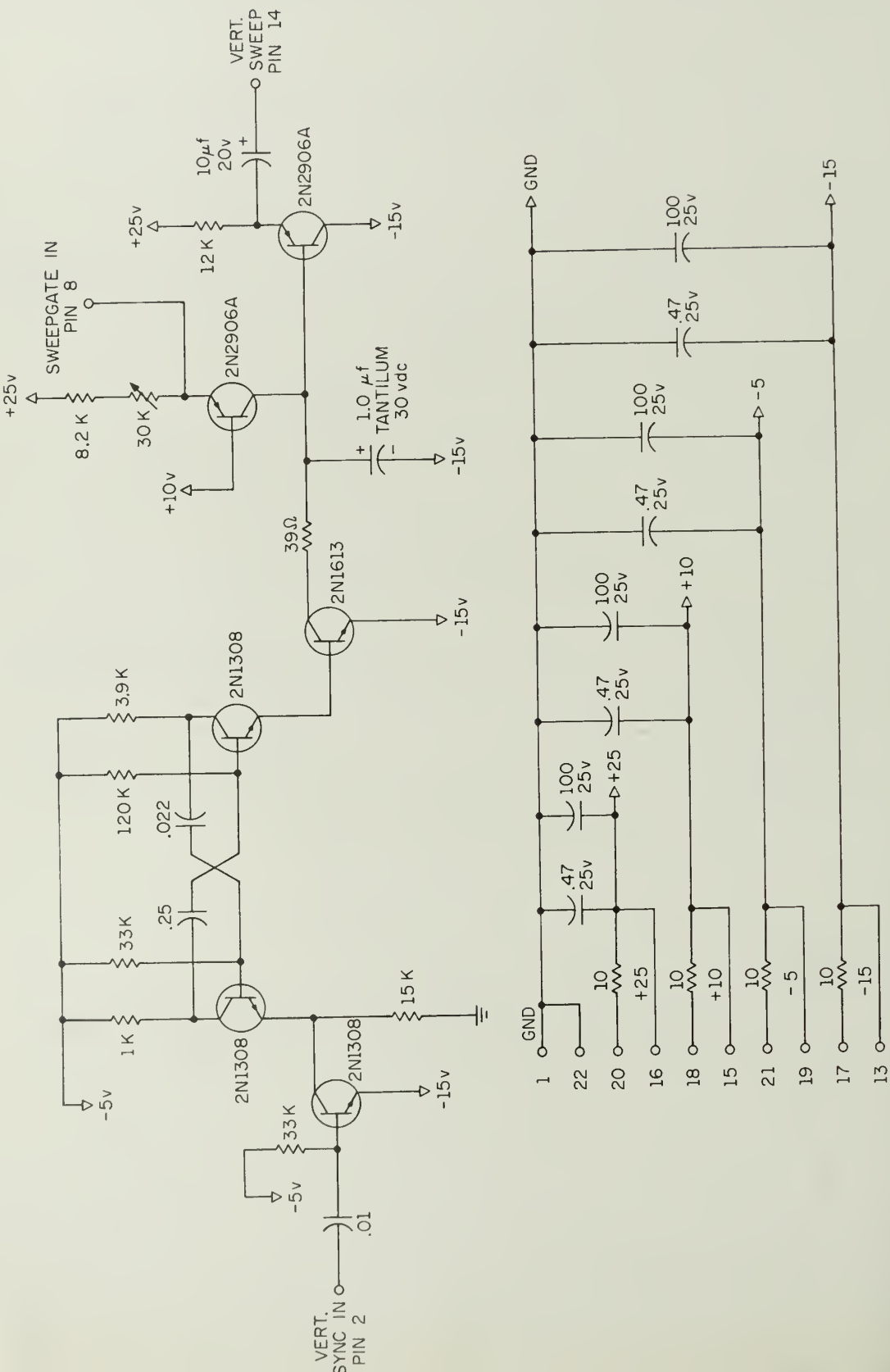
1469-110 SYNC SEPARATOR, GATE DRIVER, VERT. BLANKING LOGIC DRIVER



NOTES

1. ALL RESISTORS 1/4 W, 5% UNLESS SPECIFIED.

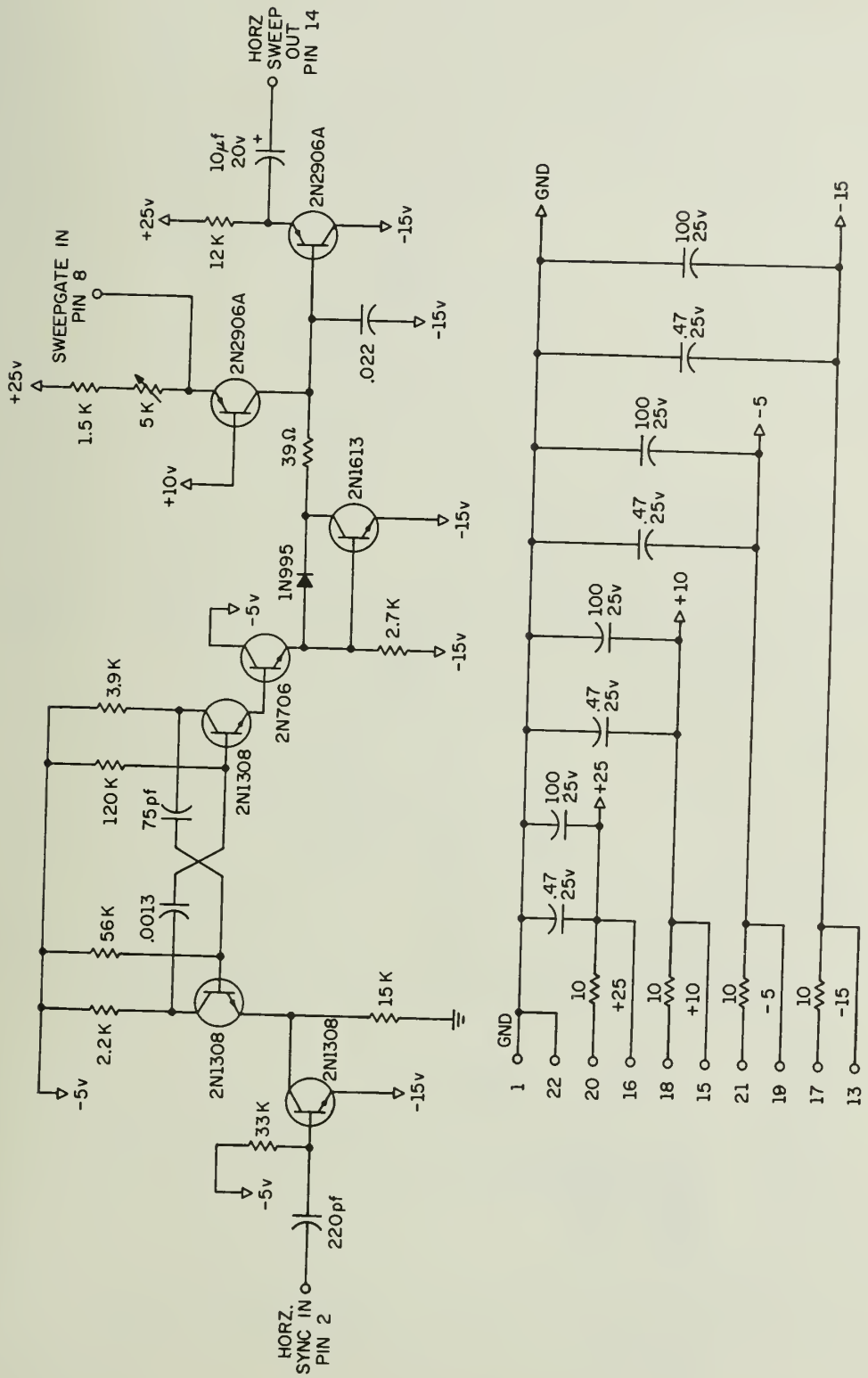
1469-111-00 VERTICAL SWEEP GENERATOR



NOTES

1. ALL RESISTORS 1/4 W, 5% UNLESS SPECIFIED.

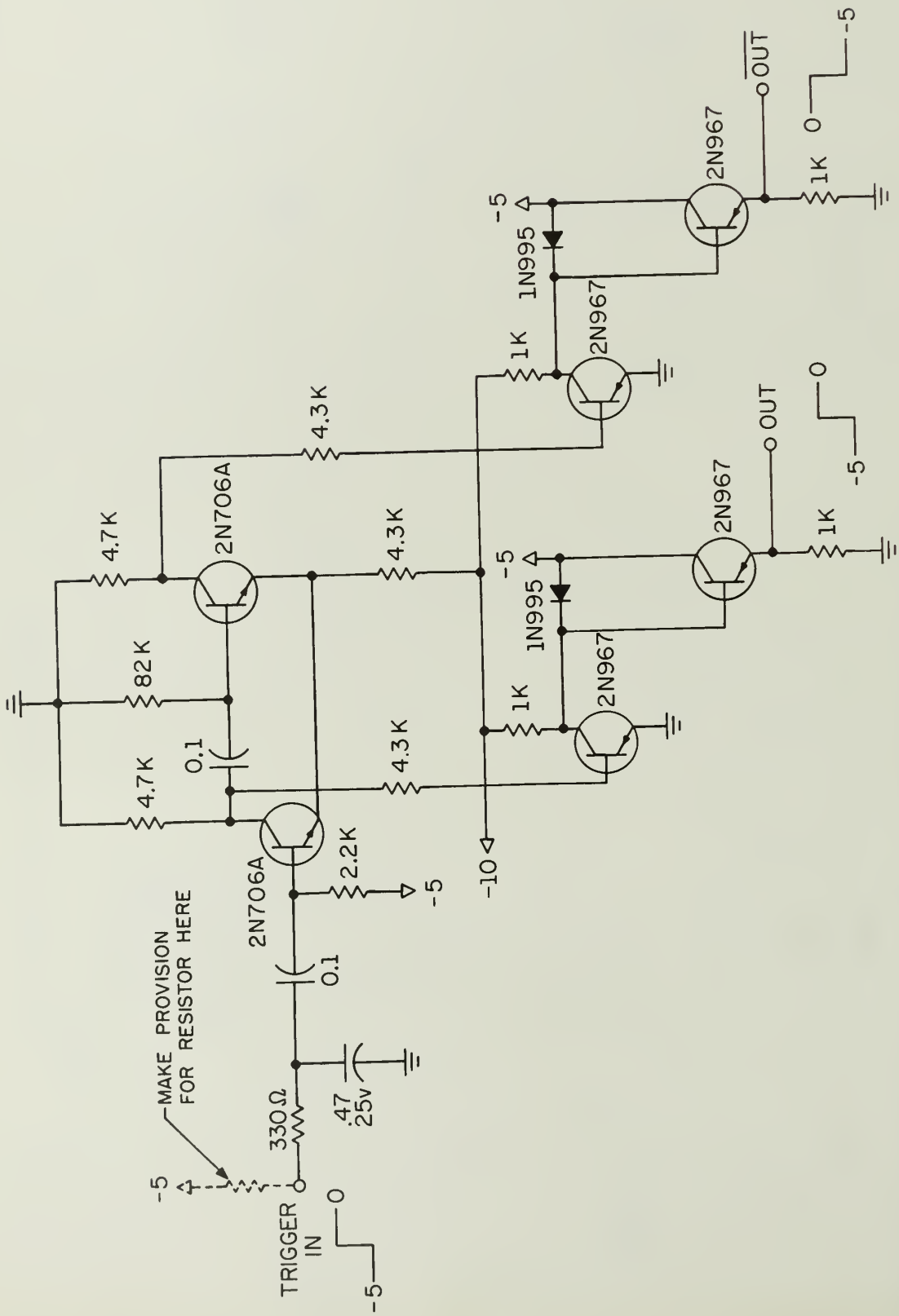
1469-111-01 HORIZONTAL SWEEP GENERATOR



NOTES

1. ALL RESISTORS 1/4 W, 5% UNLESS SPECIFIED.

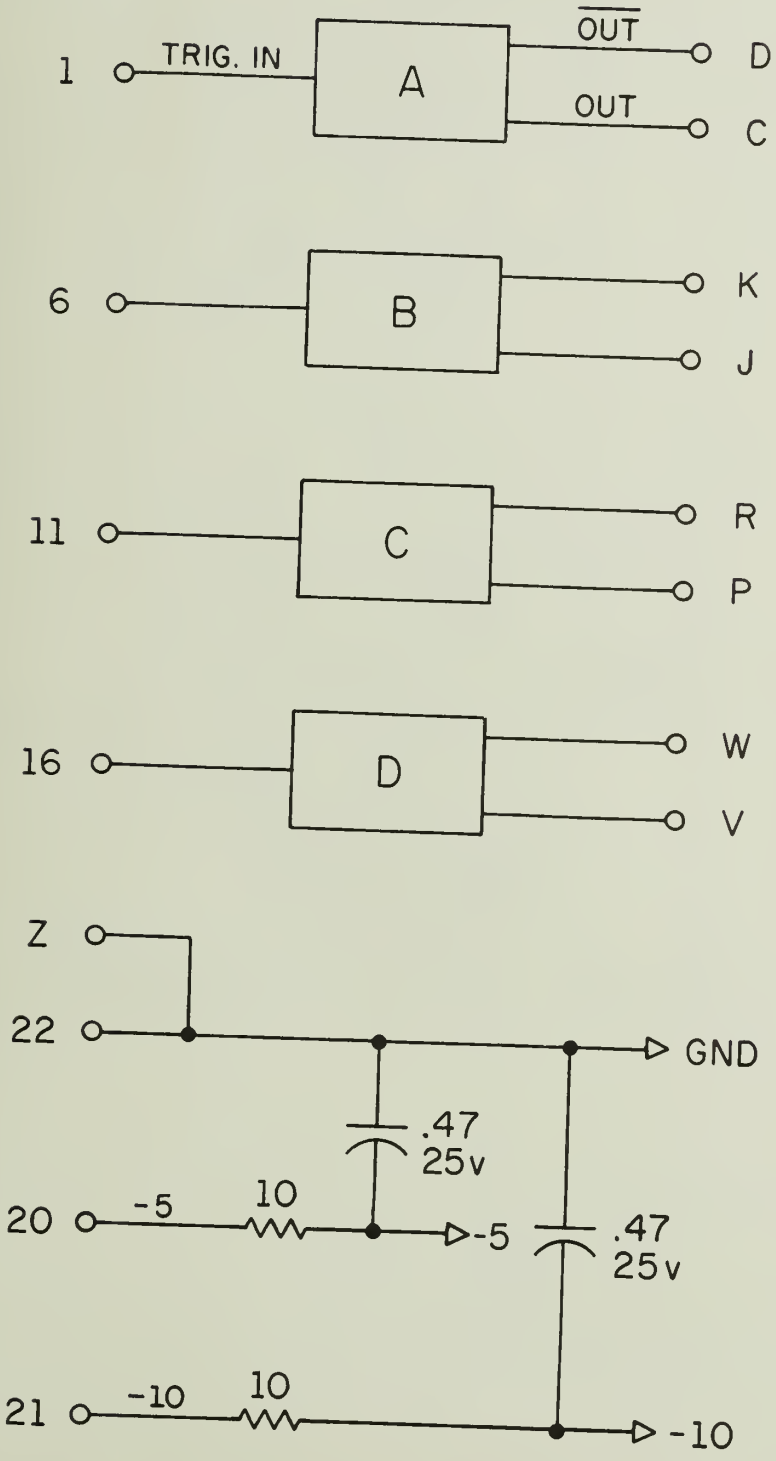
1469-112 ONE SHOT BUFFER (2 ms)



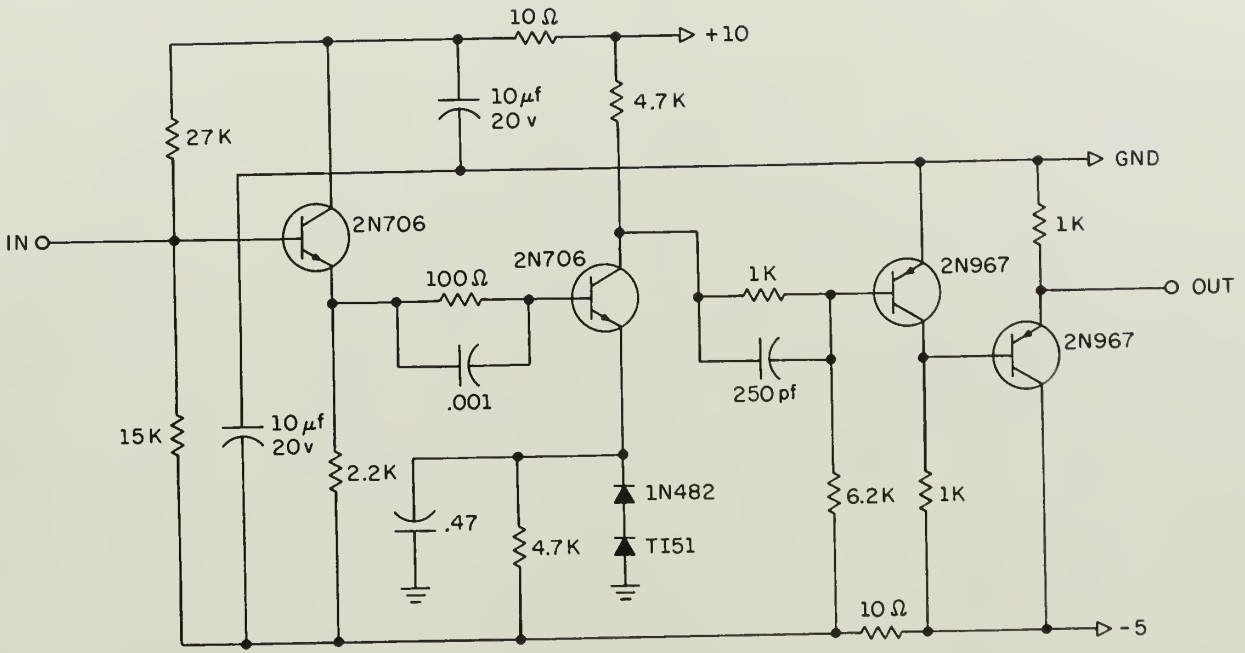
NOTES

1. ALL RESISTORS 1/4 W, 5% UNLESS SPECIFIED.
2. SEE NEXT PAGE FOR PIN CONNECTIONS.

1469-112 ONE SHOT BUFFER (2 ms)



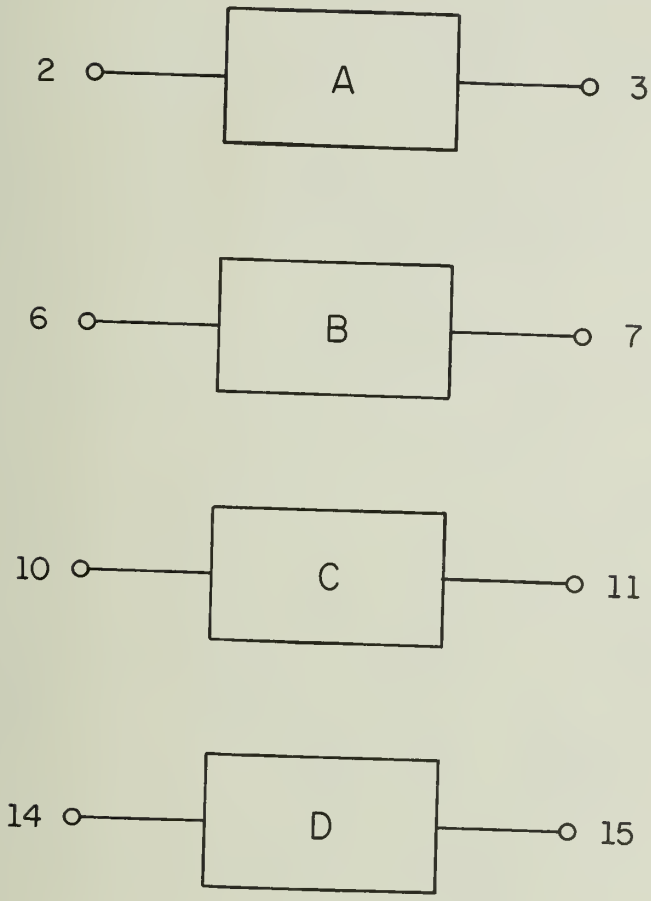
1469-113 VIDEO TO LOGIC CONVERTER

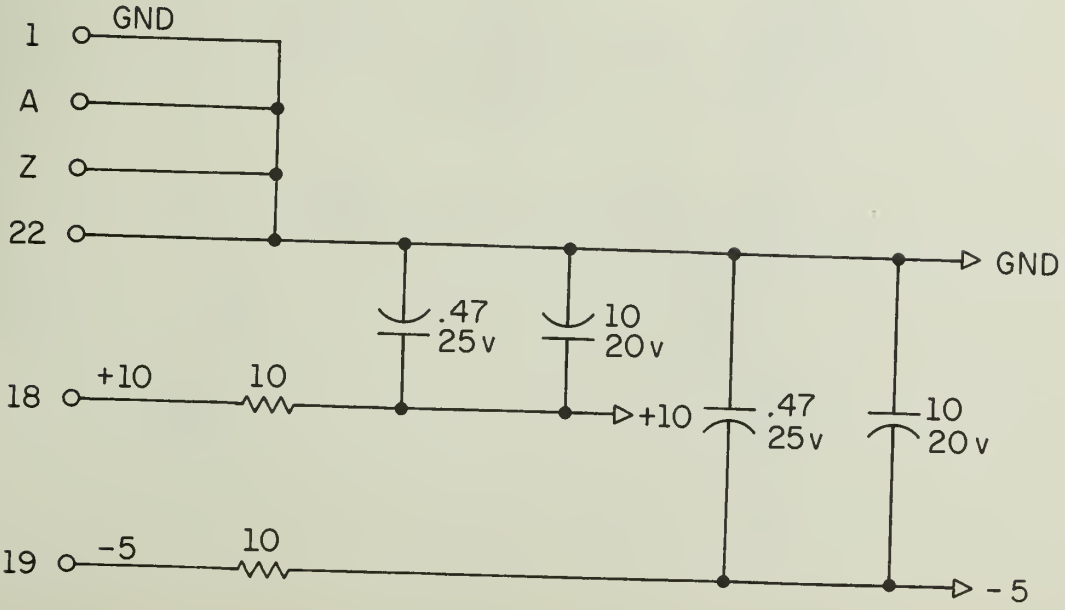


NOTES

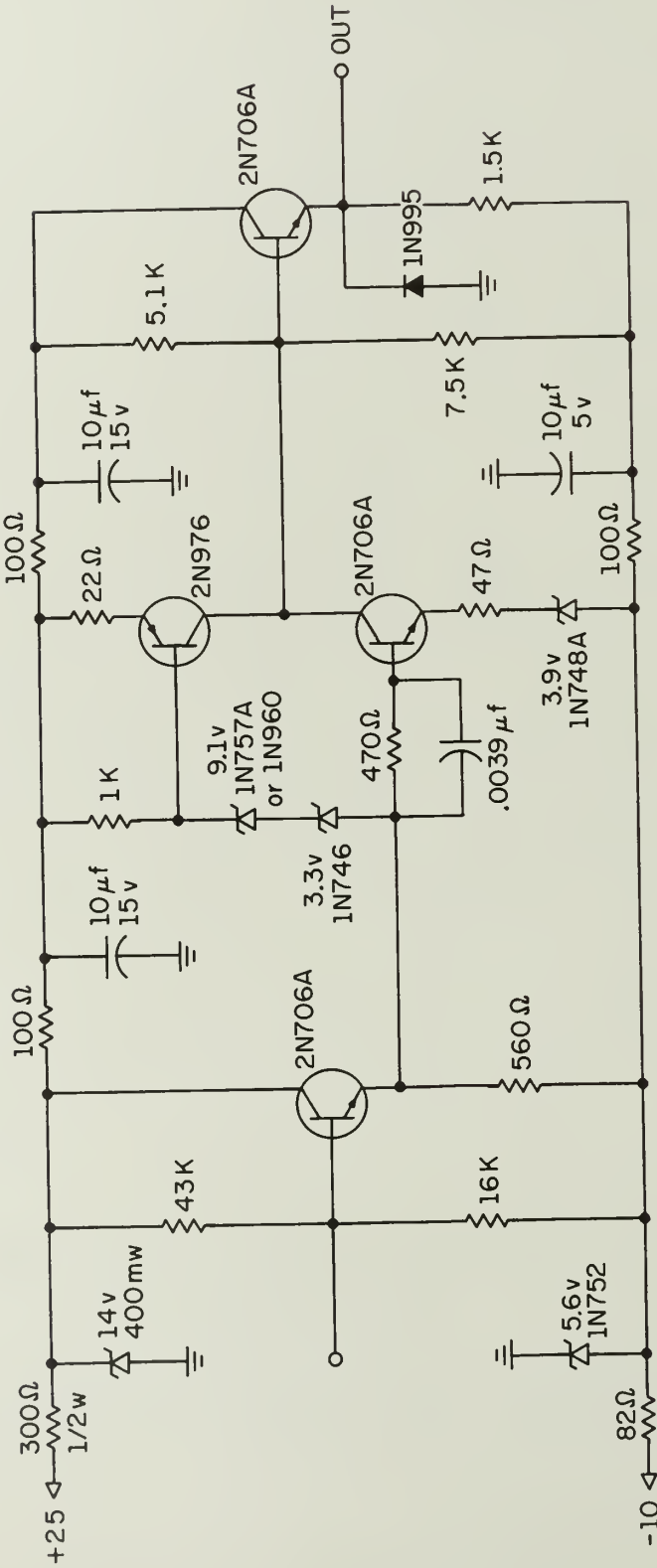
1. ALL RESISTORS 1/4 W, 5 % UNLESS SPECIFIED.
2. SEE NEXT PAGE FOR PIN CONNECTIONS.

1469-113 VIDEO TO LOGIC CONVERTER





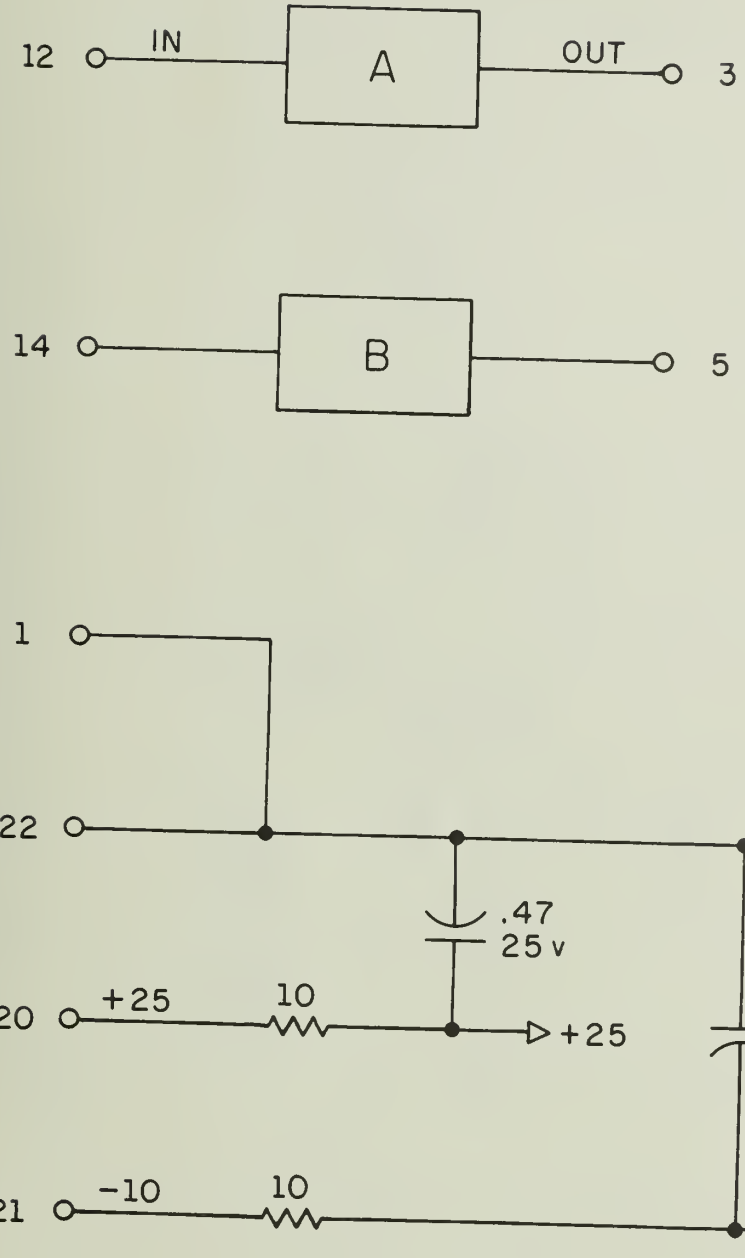
1469-114 Z-AXIS DRIVER



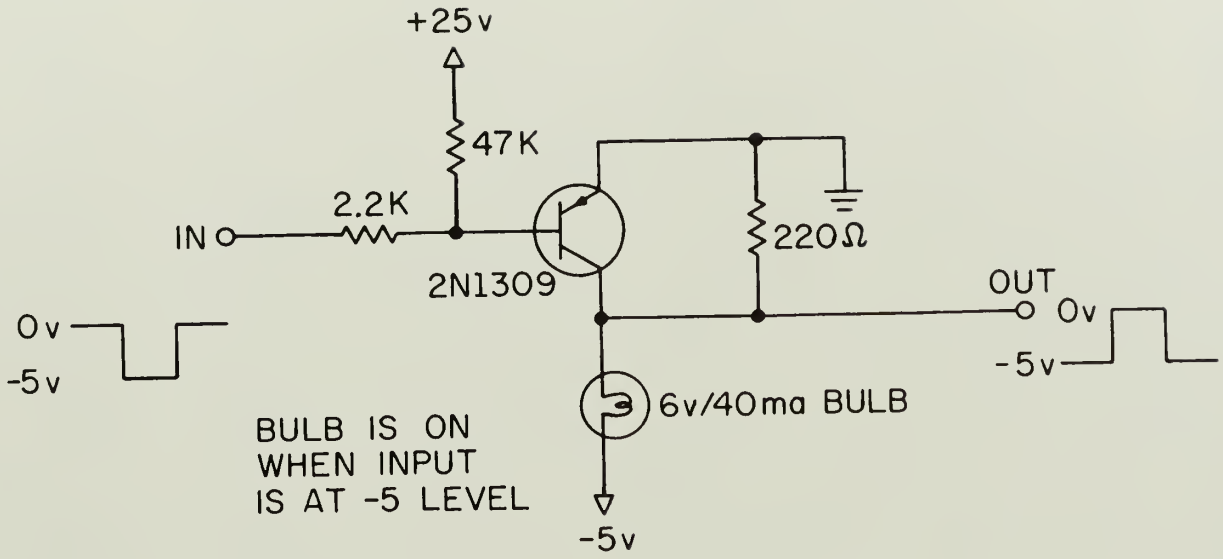
NOTES

1. ALL RESISTORS 1/4 w, 5% UNLESS SPECIFIED.
2. SEE NEXT PAGE FOR PIN CONNECTIONS.

1469-114 Z-AXIS DRIVER



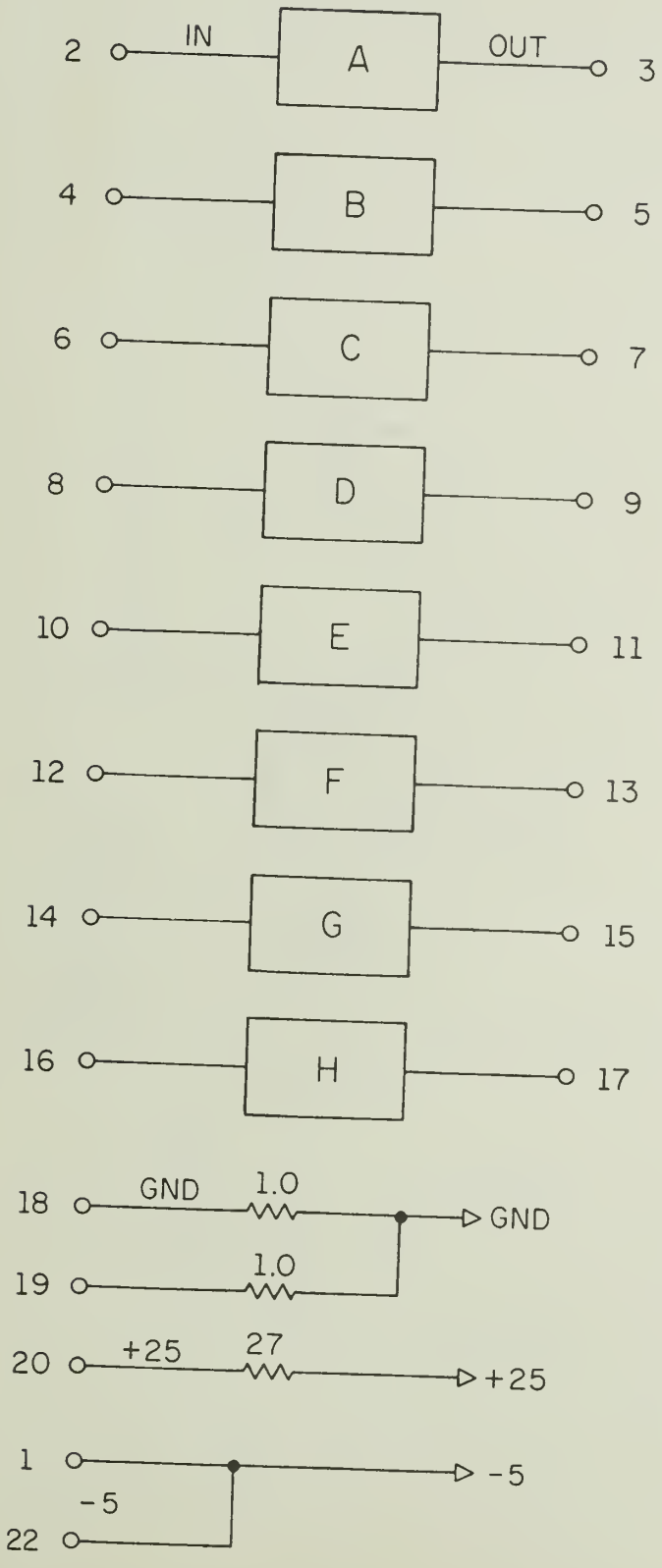
1469-115-03 INDICATOR DRIVER



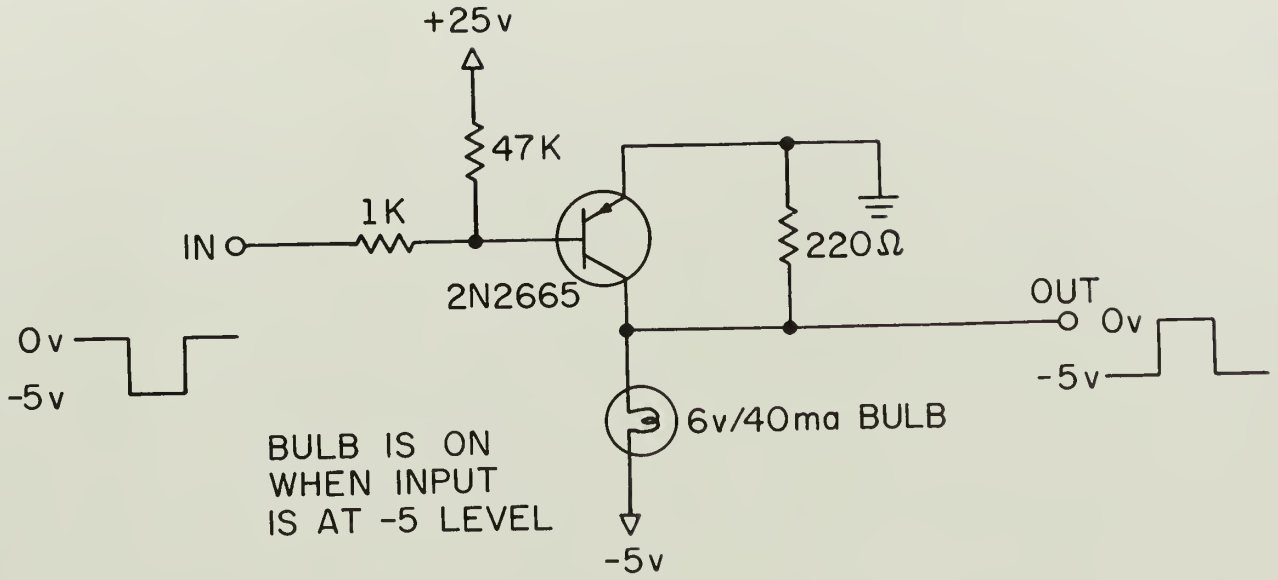
NOTES

1. ALL RESISTORS 1/4w, 5% UNLESS SPECIFIED.
2. SEE NEXT PAGE FOR PIN CONNECTIONS.

1469-115-03 INDICATOR DRIVER



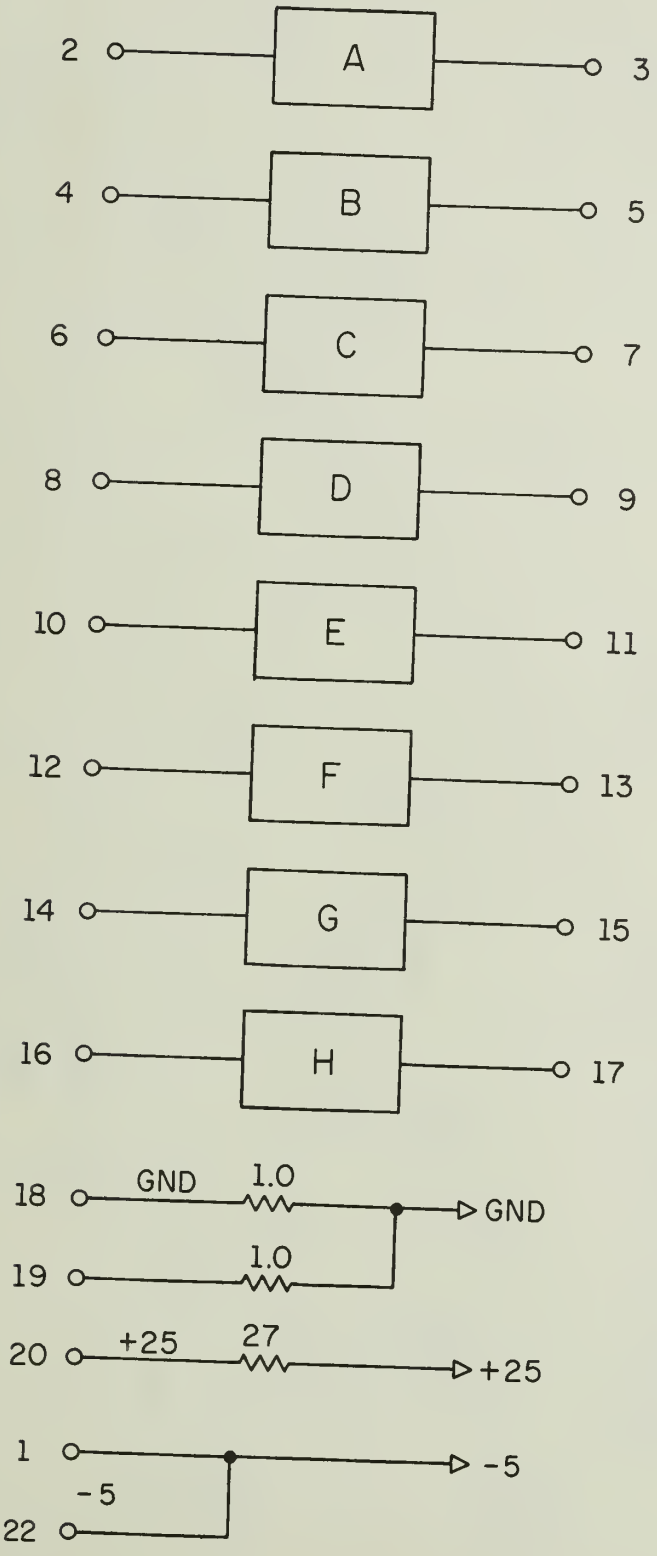
1469-115-04 INDICATOR DRIVER



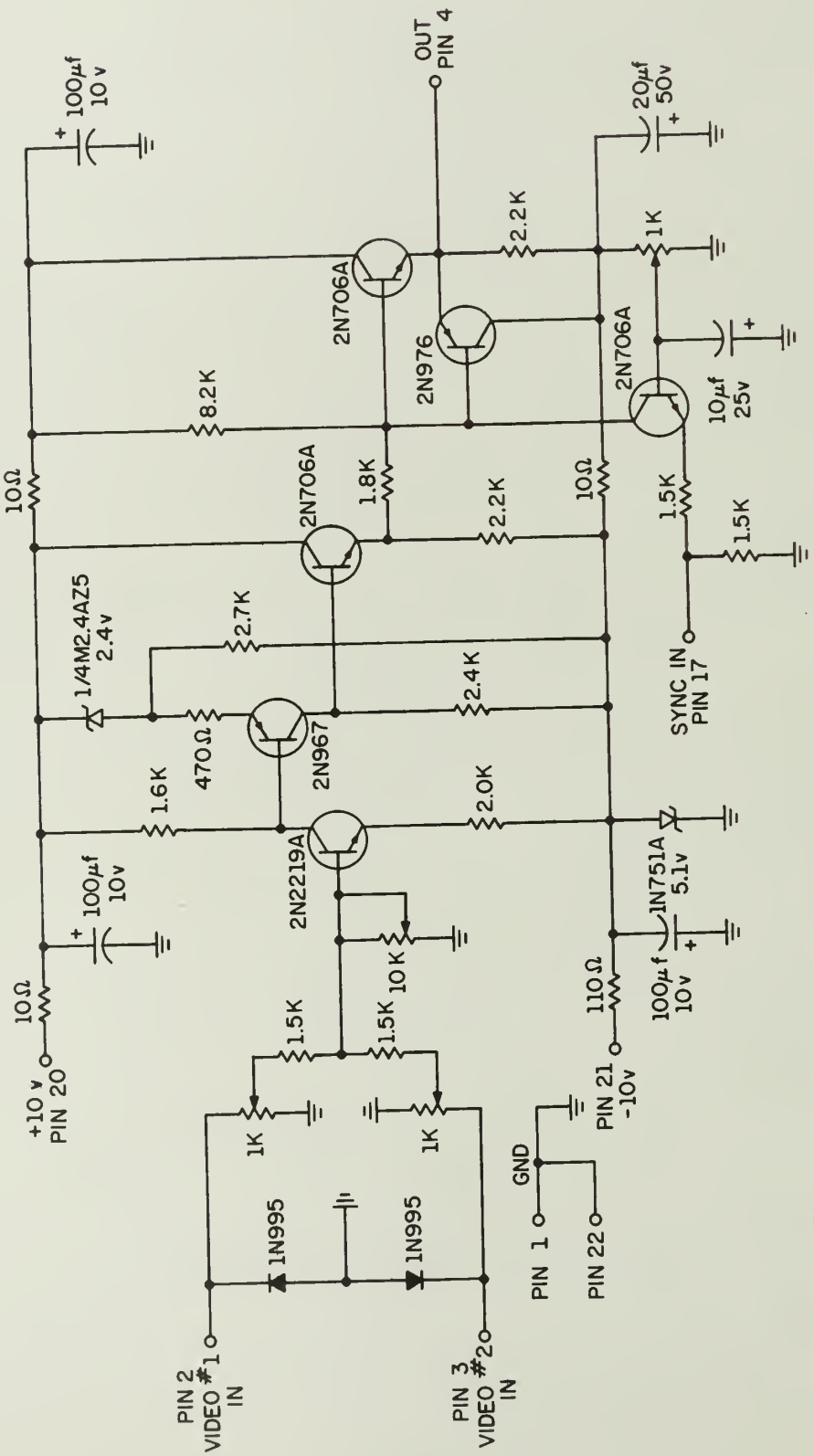
NOTES

1. ALL RESISTORS 1/4w, 5% UNLESS SPECIFIED.
2. SEE NEXT PAGE FOR PIN CONNECTIONS.

1469-115-04 INDICATOR DRIVER



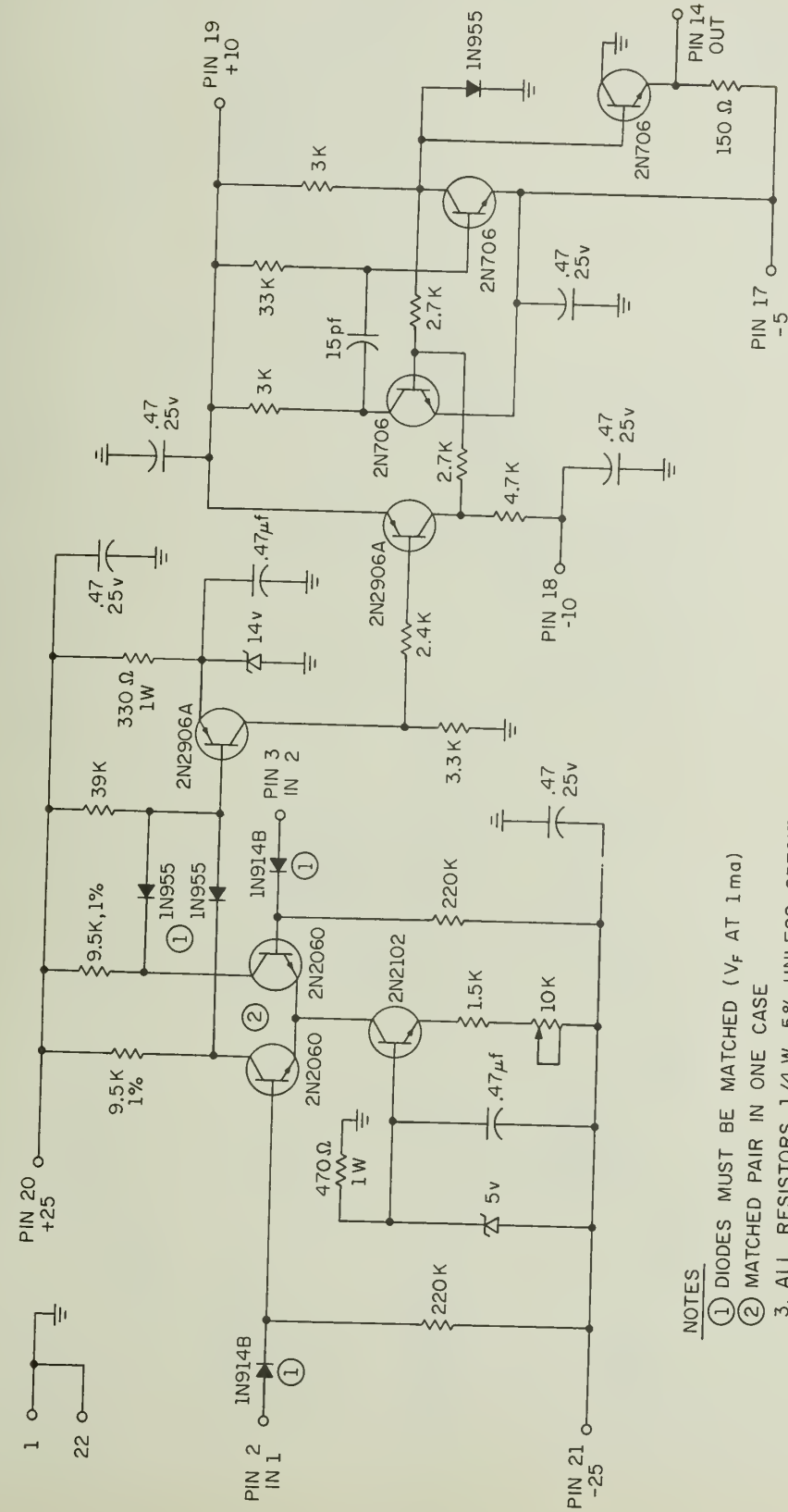
1469-116 VIDEO ADDER AND SYNC INSERTER



NOTES

1. ALL RESISTORS 1/4 w, 5% UNLESS SPECIFIED.

1469-117 COMPARATOR



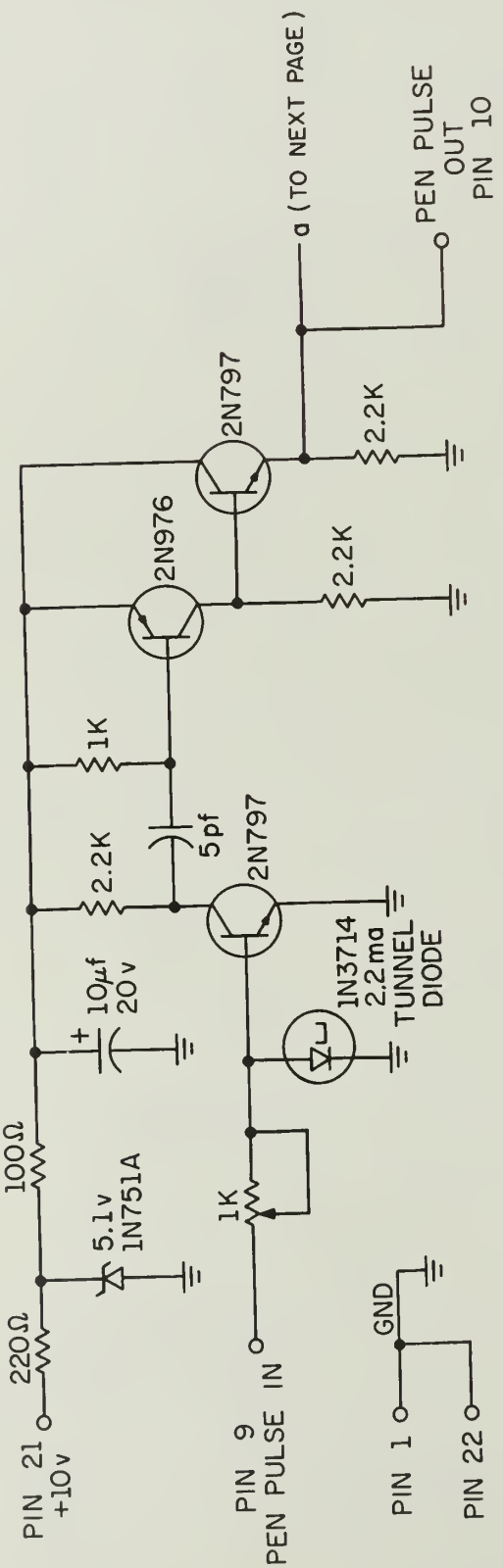
NOTES

① DIODES MUST BE MATCHED (V_F AT 1 ma)

② MATCHED PAIR IN ONE CASE

3. ALL RESISTORS 1/4 W, 5% UNLESS SPECIFIED

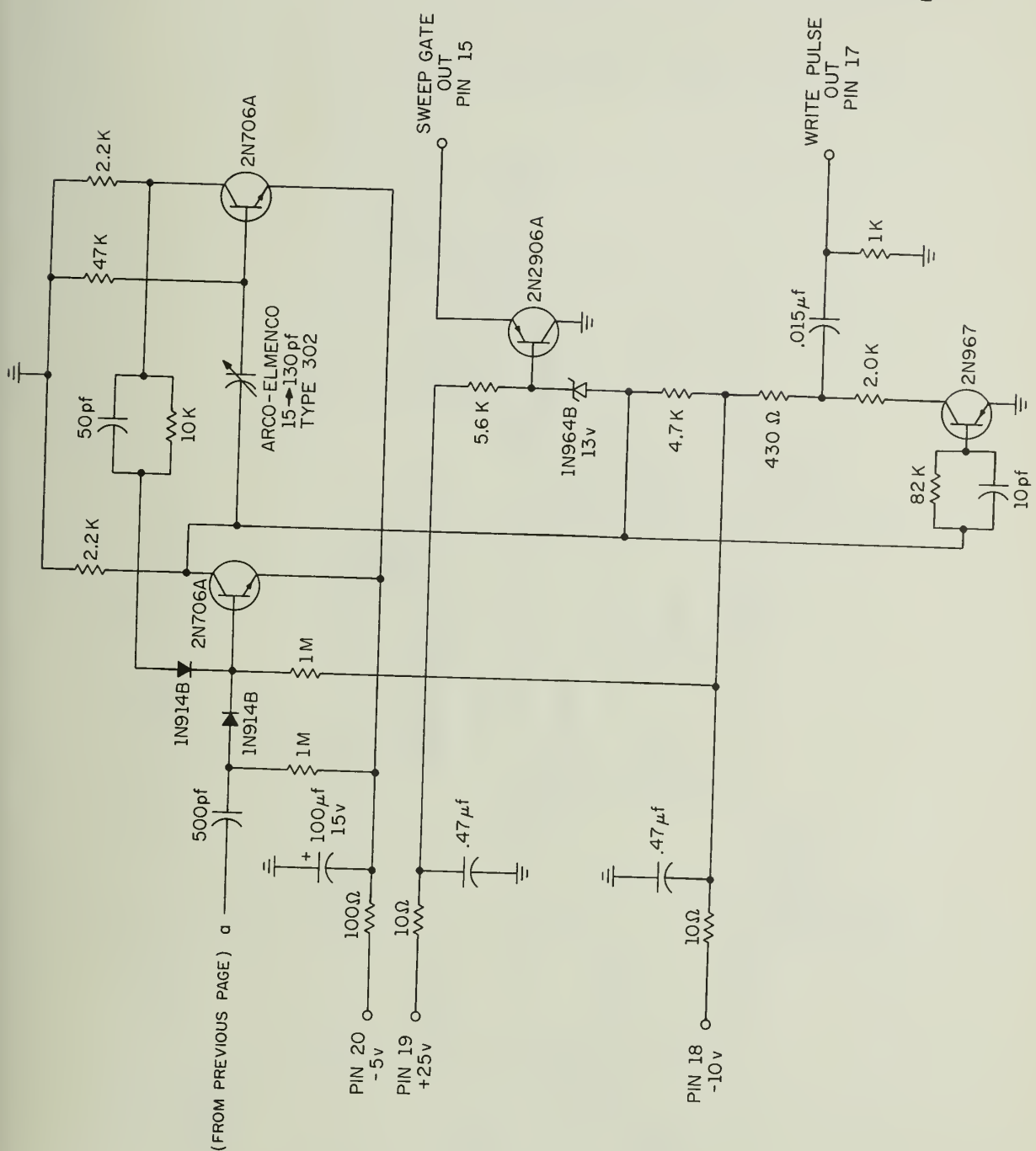
1469-118 PEN PULSE SHAPING CIRCUIT AND MULTIVIBRATOR GATE



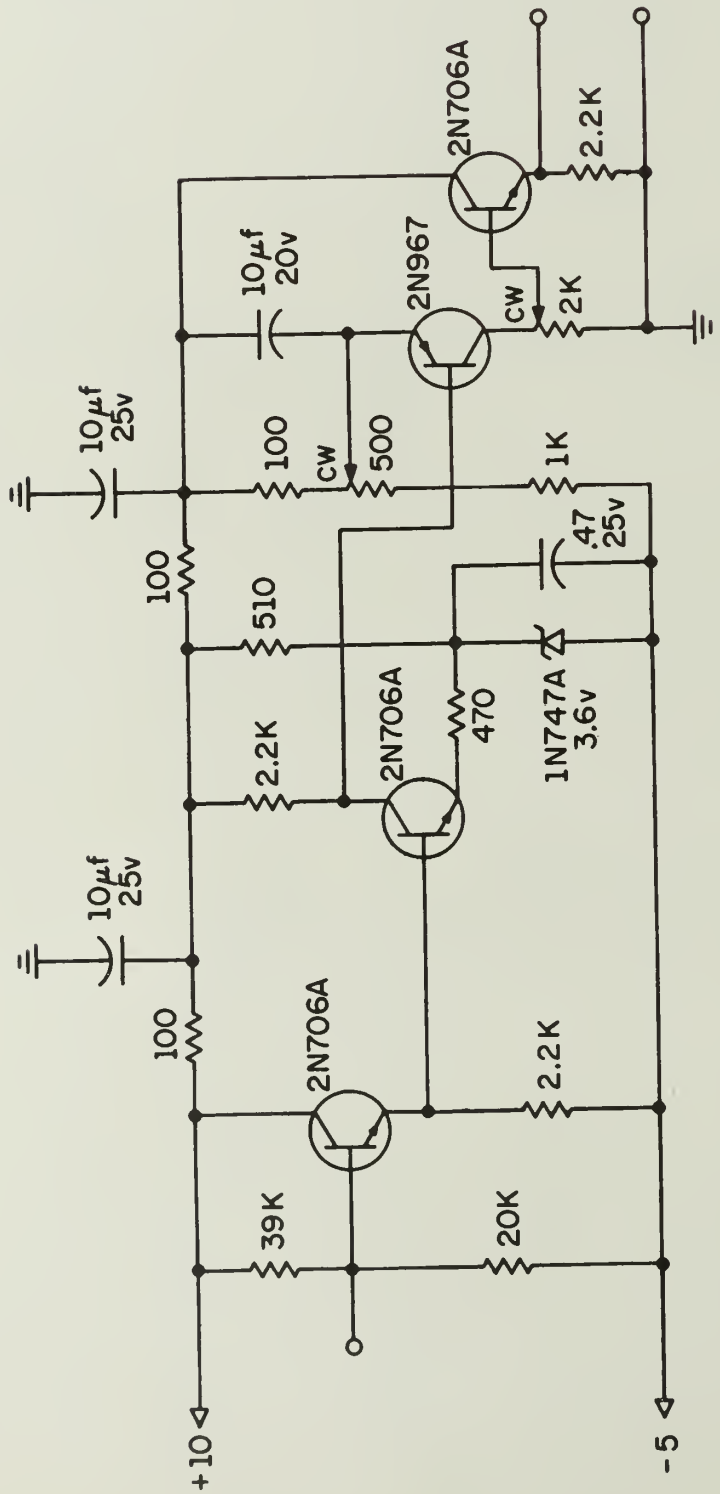
NOTES

1. ALL RESISTORS 1/4 w, 5%

1469-118 PEN PULSE SHAPING CIRCUIT AND MULTIVIBRATOR GATE



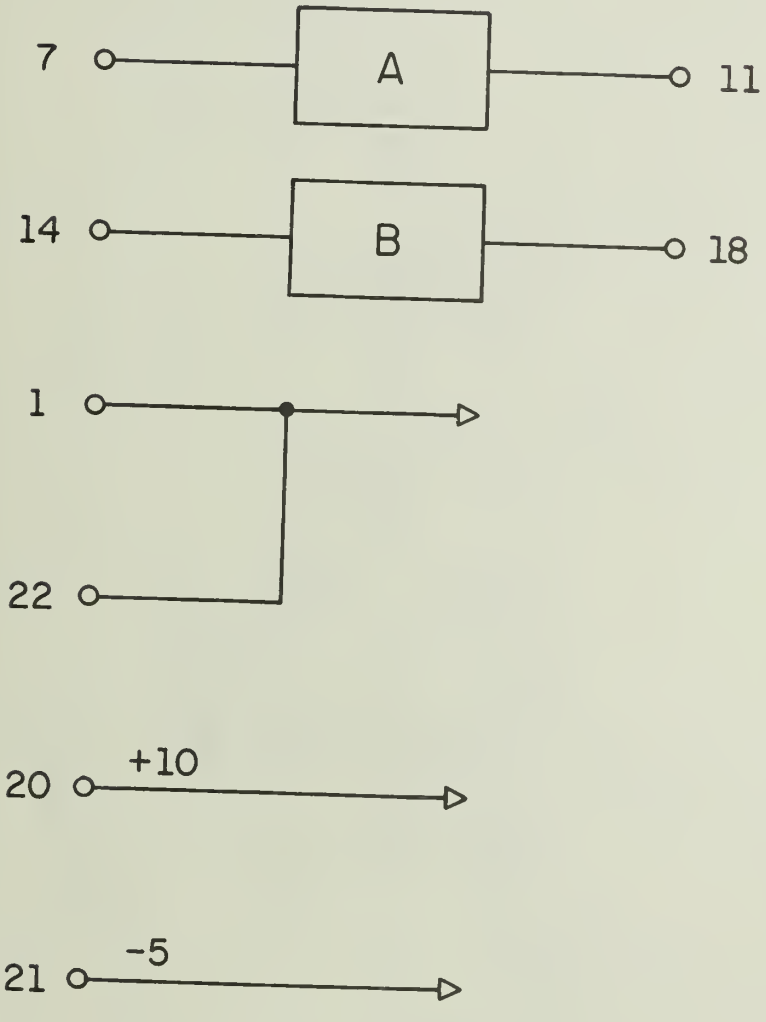
1469-119 DISCRIMINATOR AND SHAPER



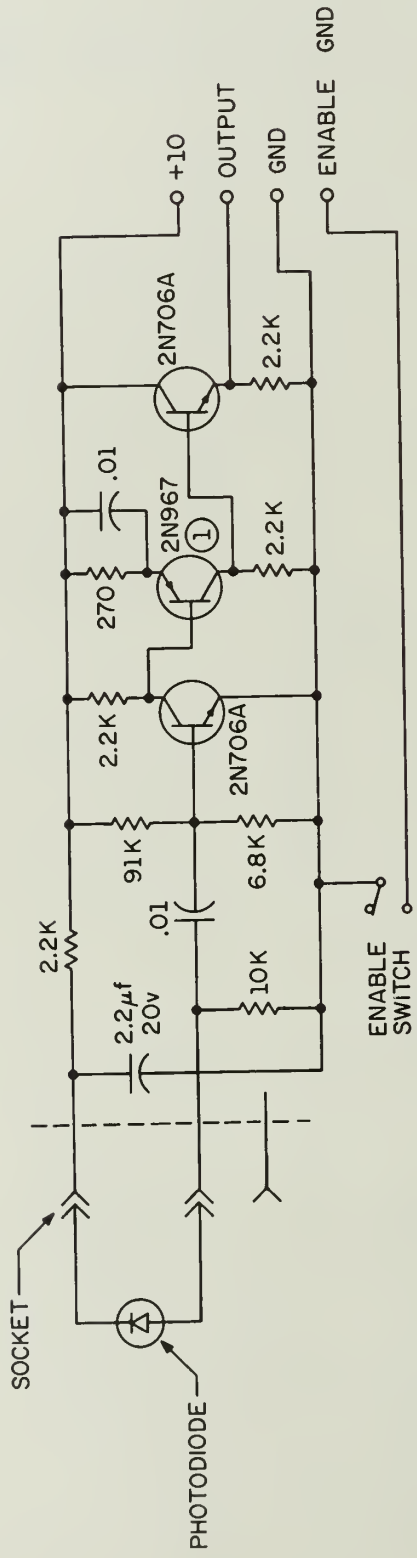
NOTES

1. ALL RESISTORS 1/4 w, 5% UNLESS SPECIFIED.
2. FOR PIN CONNECTIONS SEE NEXT PAGE.

1469-119 DISCRIMINATOR AND SHAPER

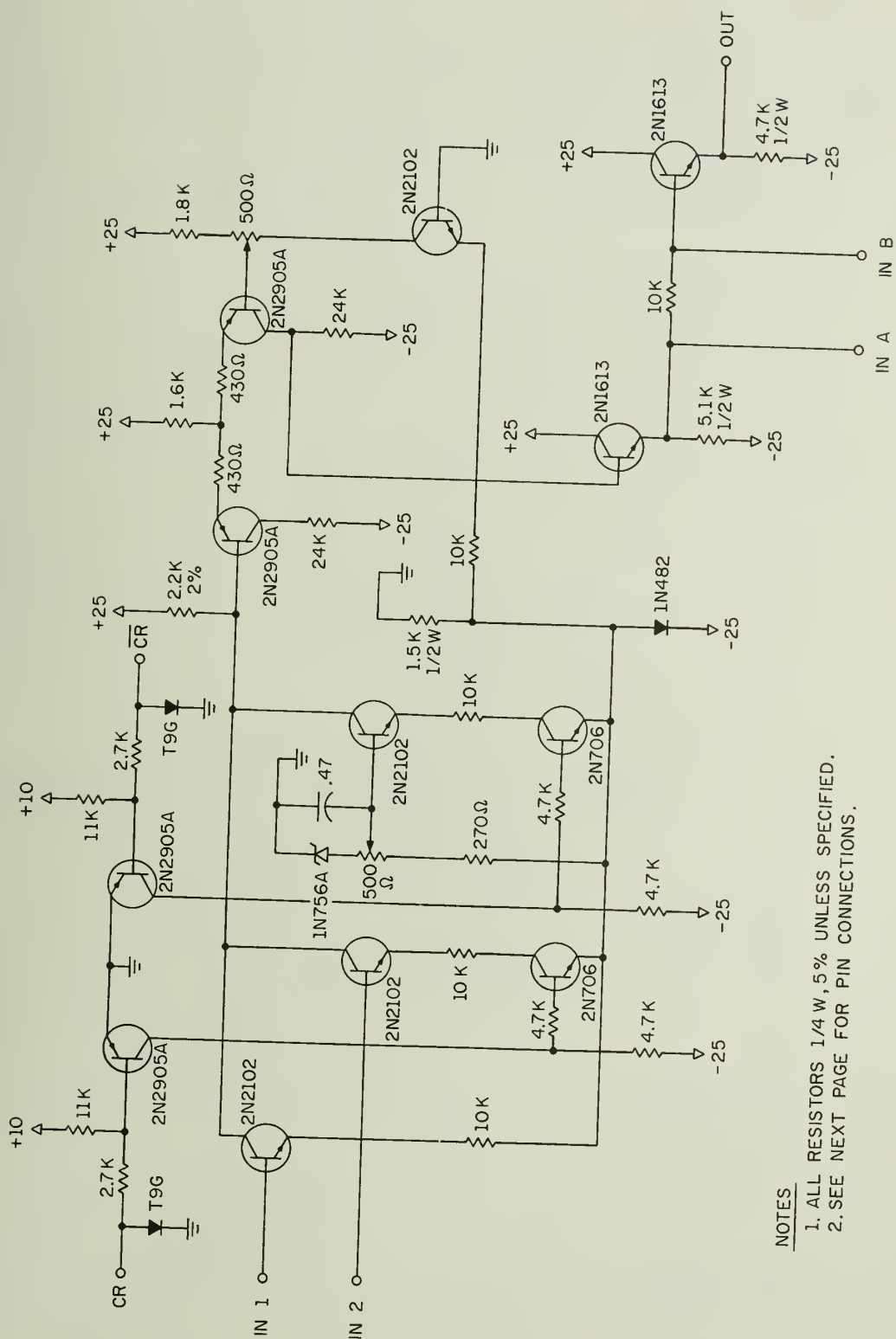


1469-121 PEN PREAMPLIFIER



NOTES
1. MIN. β OF 150
2. ALL RESISTORS 1/8 w, 5 % UNLESS SPECIFIED.

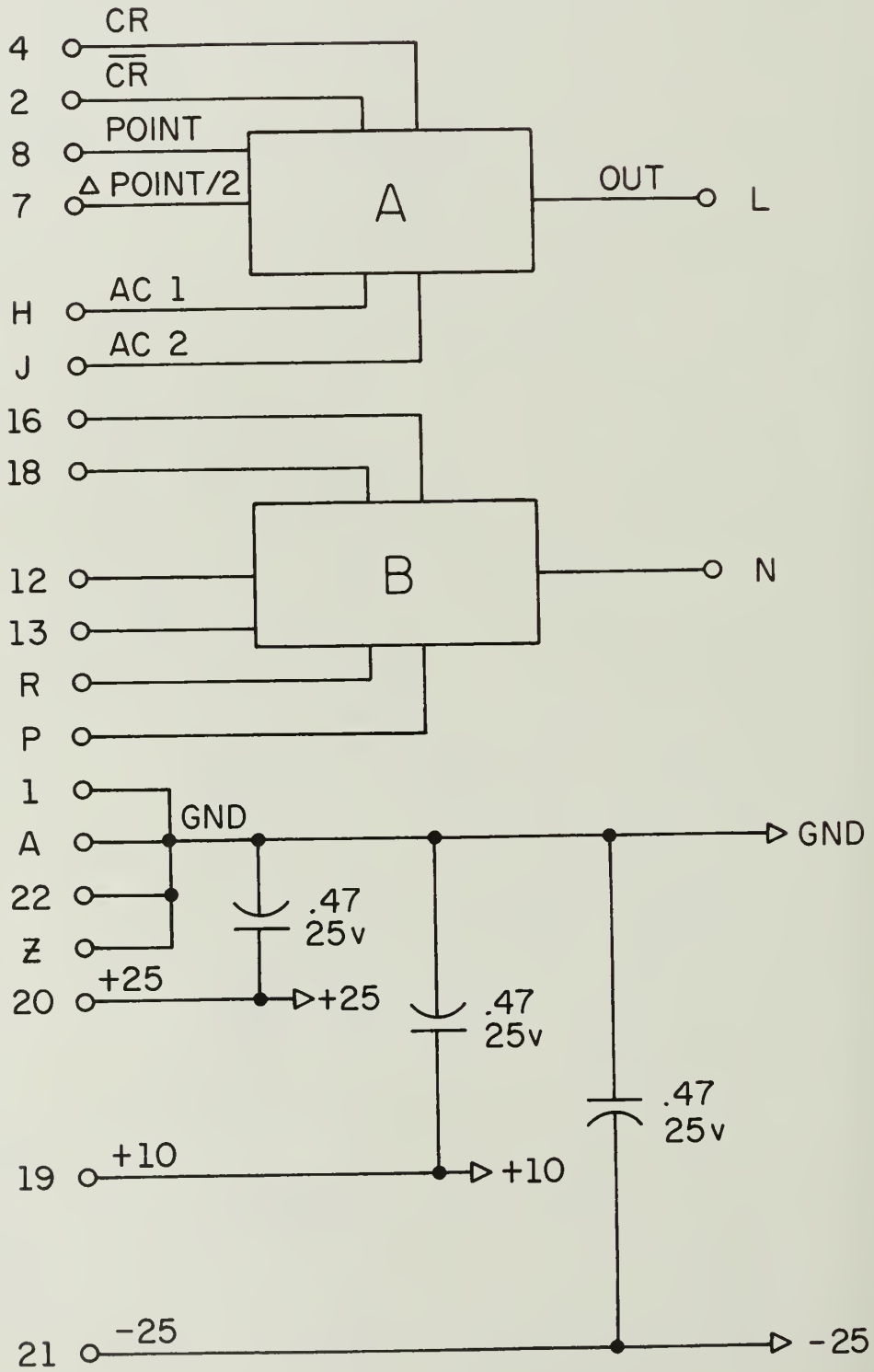
1469-123 DC MIXER AND AMPLIFIER



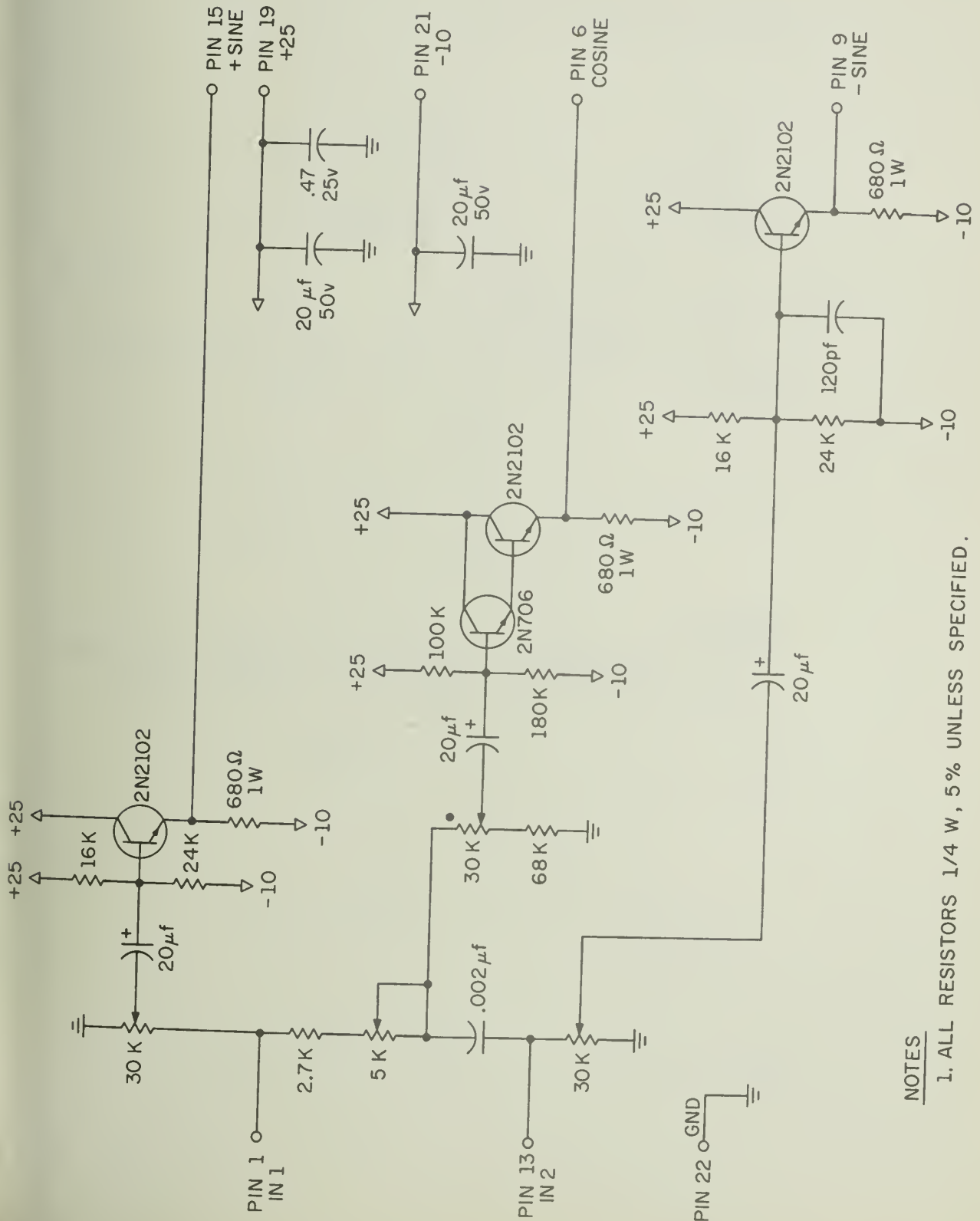
NOTES

1. ALL RESISTORS 1/4 W, 5% UNLESS SPECIFIED.
2. SEE NEXT PAGE FOR PIN CONNECTIONS.

1469-123 DC MIXER AND AMPLIFIER



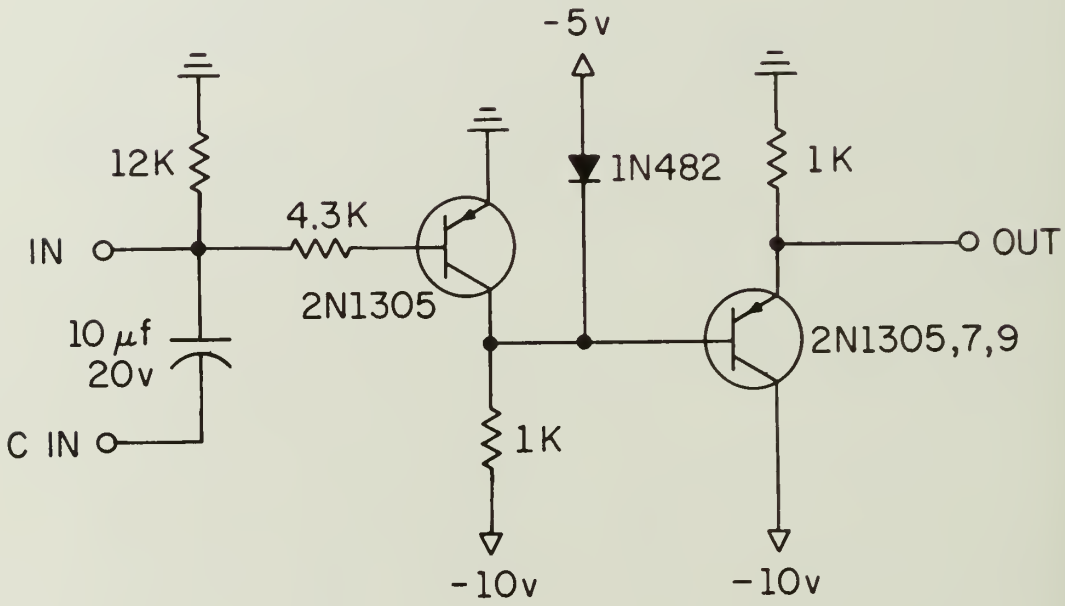
1469-152-00 PHASE SHIFTER AND EMITTER FOLLOWER



NOTES

1. ALL RESISTORS 1/4 W, 5% UNLESS SPECIFIED.

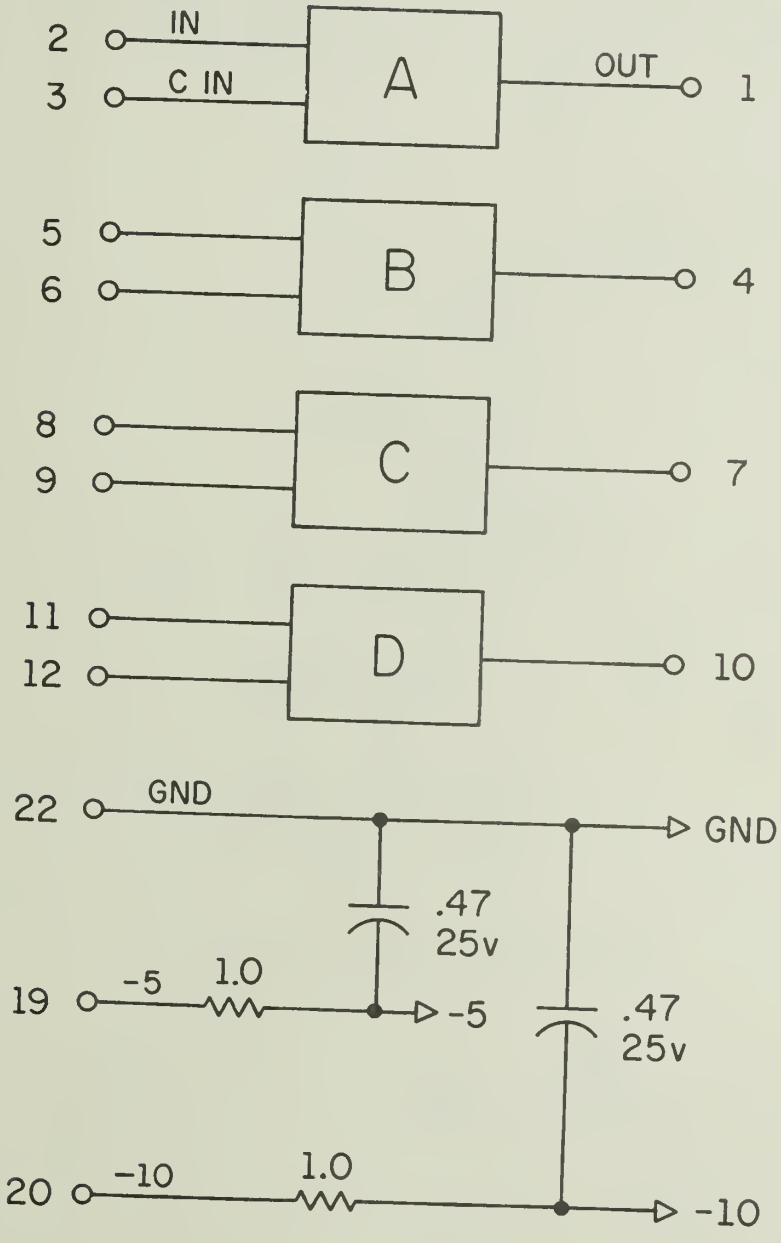
1469-152-01 EMITTER FOLLOWER



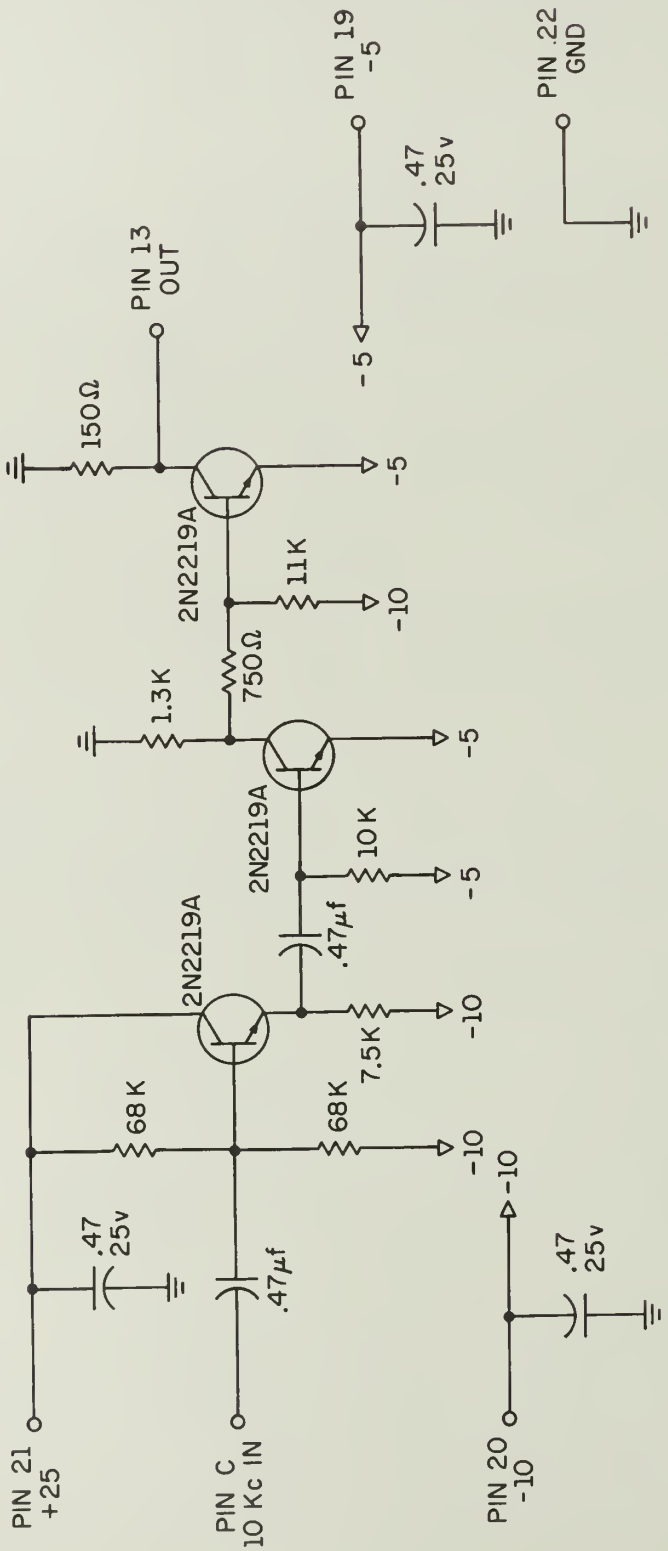
NOTES

1. ALL RESISTORS 1/4 W, 5% UNLESS SPECIFIED.
2. SEE NEXT PAGE FOR PIN CONNECTIONS.

1469-152-01 EMITTER FOLLOWER



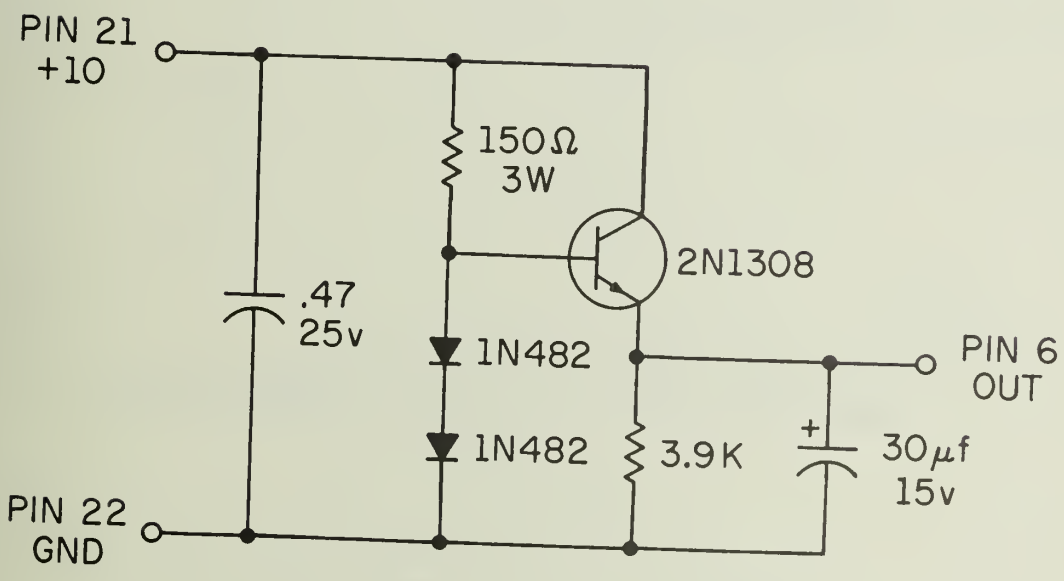
1469-152-02 10 Kc SQUAREWAVE GENERATOR



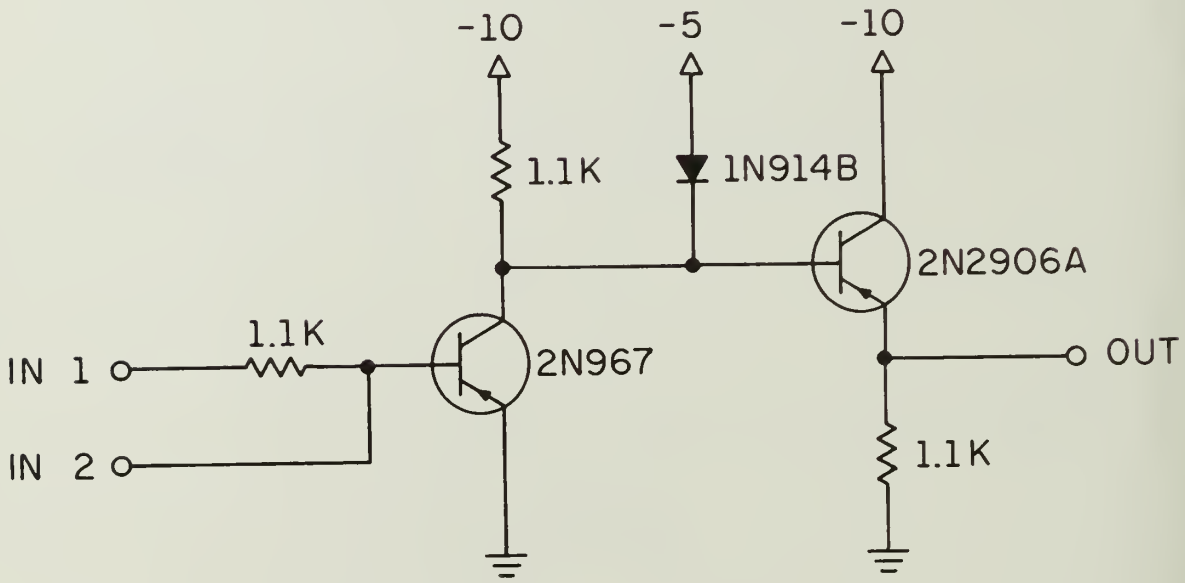
NOTES

1. ALL RESISTORS 1/4 W, 5% UNLESS SPECIFIED.

1469-152-03 +1.7 VOLT POWER SUPPLY



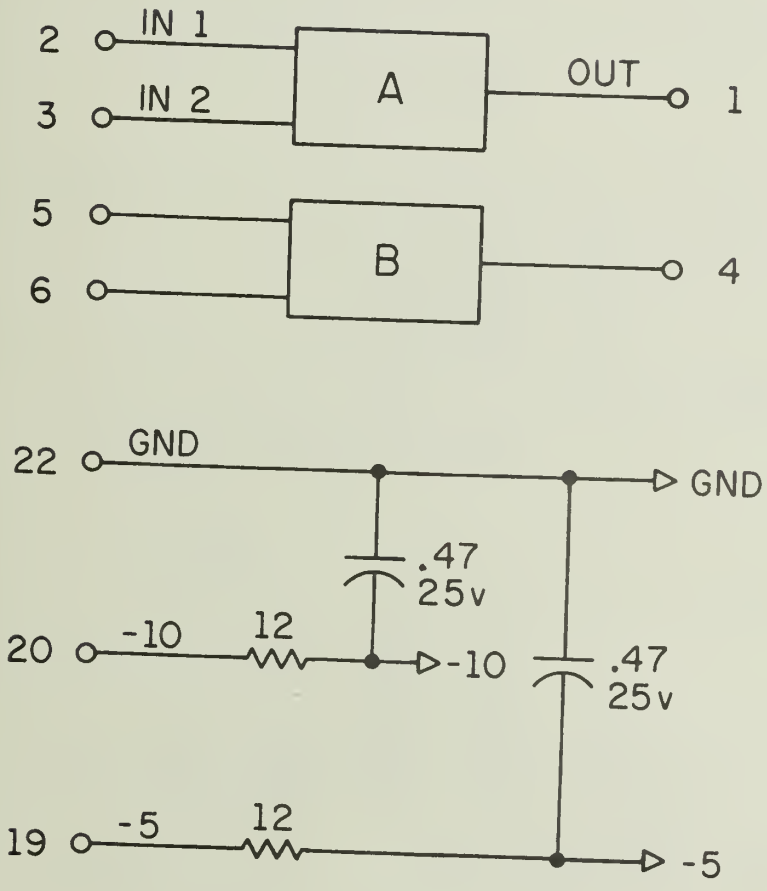
1469-152-04 EMITTER FOLLOWER



NOTES

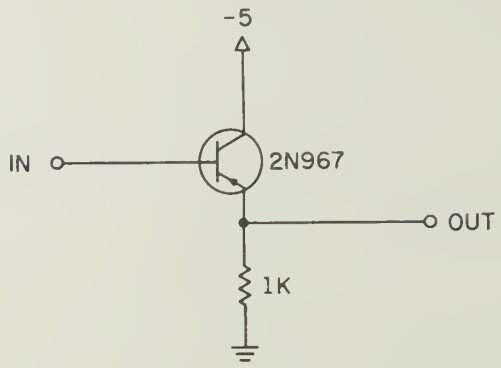
1. ALL RESISTORS 1/4 W, 5 % .
2. SEE NEXT PAGE FOR PIN CONNECTIONS.

1469-152-04 EMITTER FOLLOWER

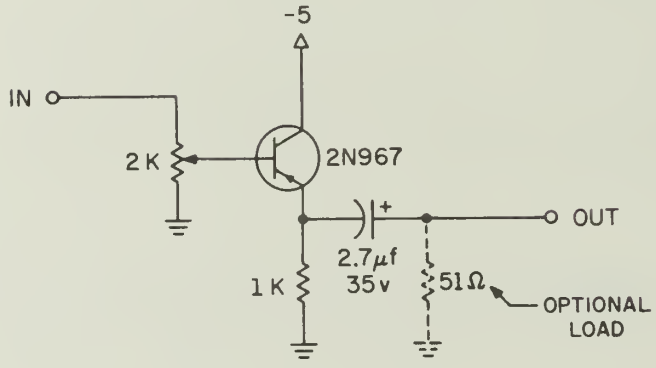


1469-152-05 EMITTER FOLLOWER

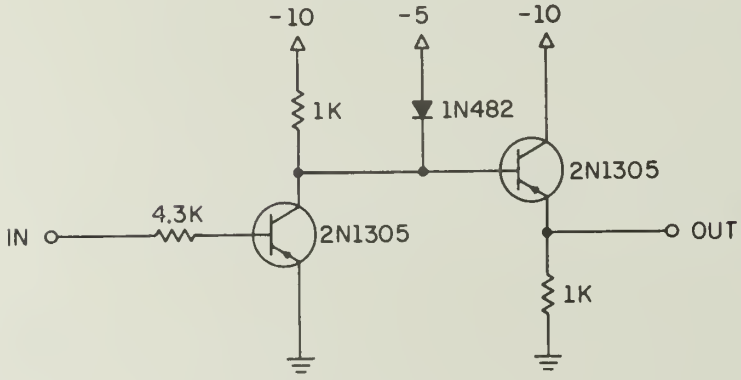
CIRCUITS A & B



CIRCUIT C



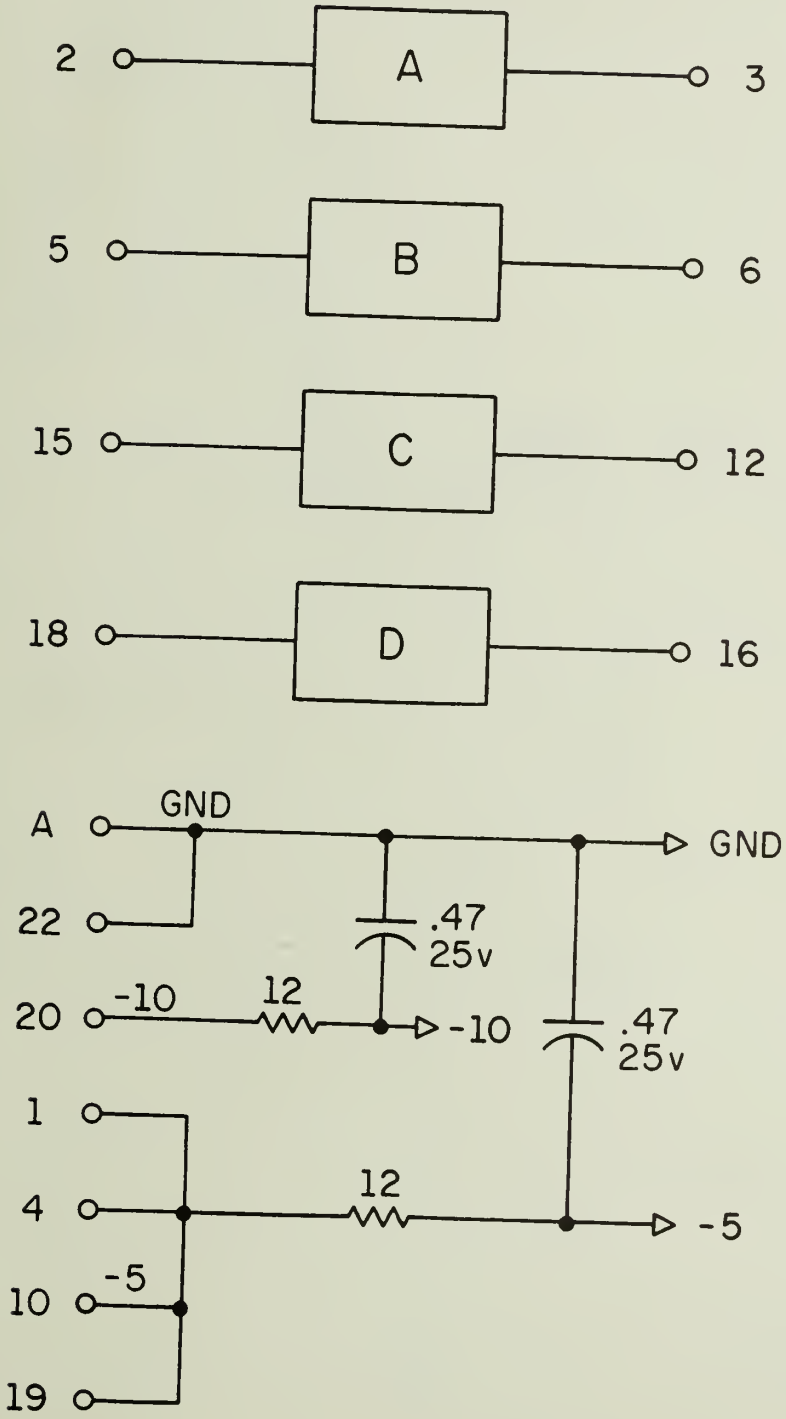
CIRCUIT D



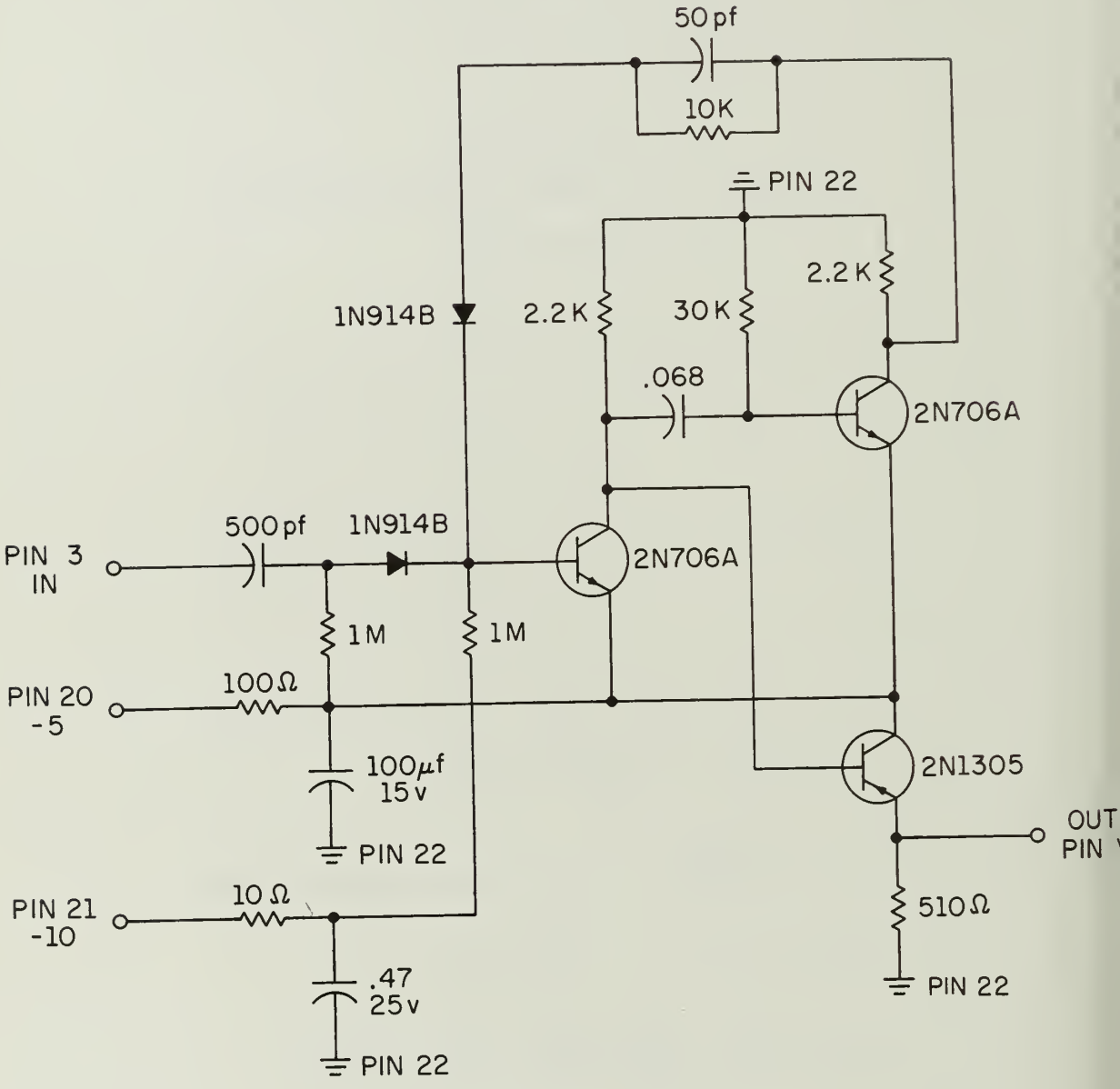
NOTES

1. ALL RESISTORS 1/4 W, 5%.
2. SEE NEXT PAGE FOR PIN CONNECTIONS.

1469-152-05 EMITTER FOLLOWER



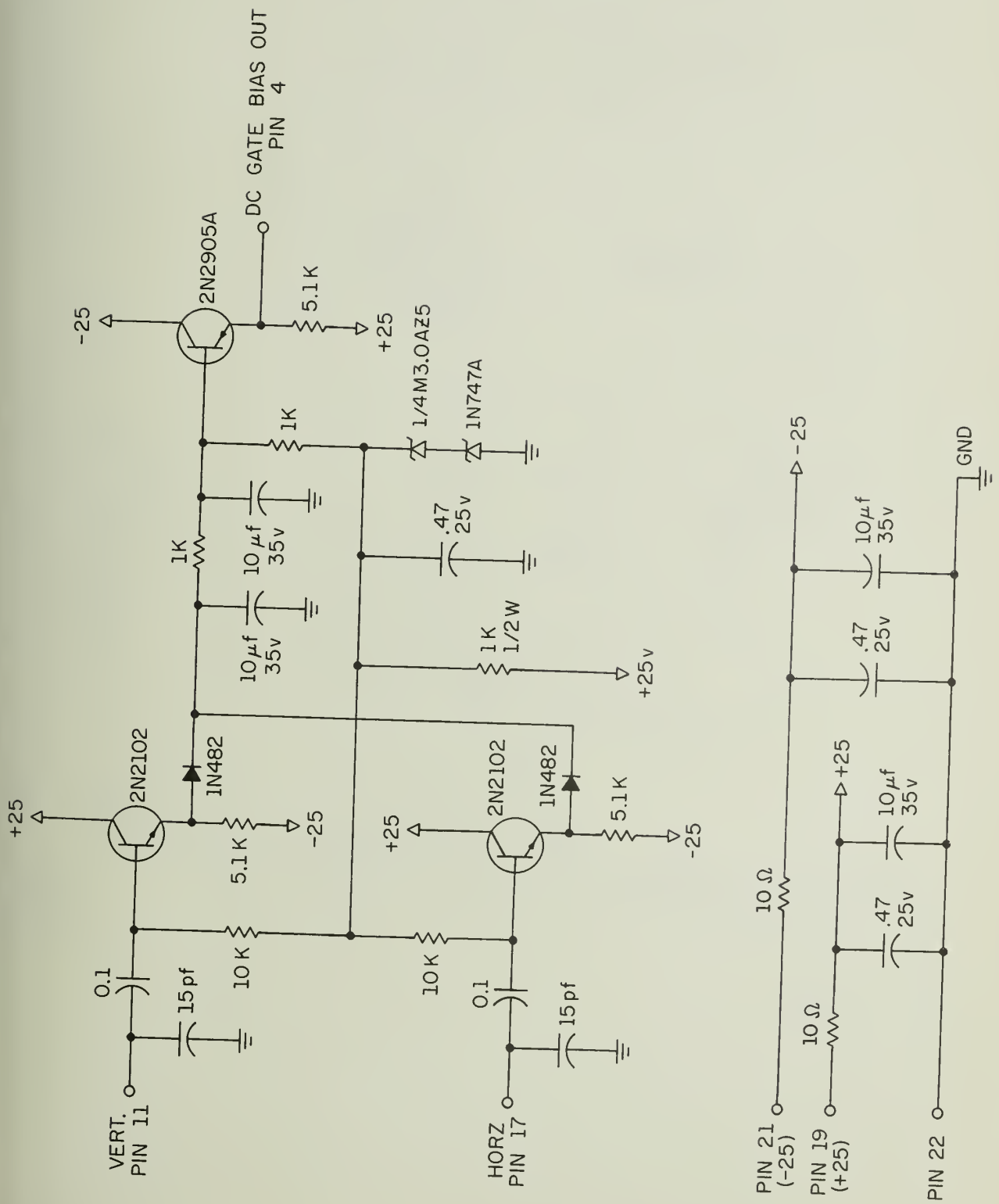
1469-152-06 PEN GATE



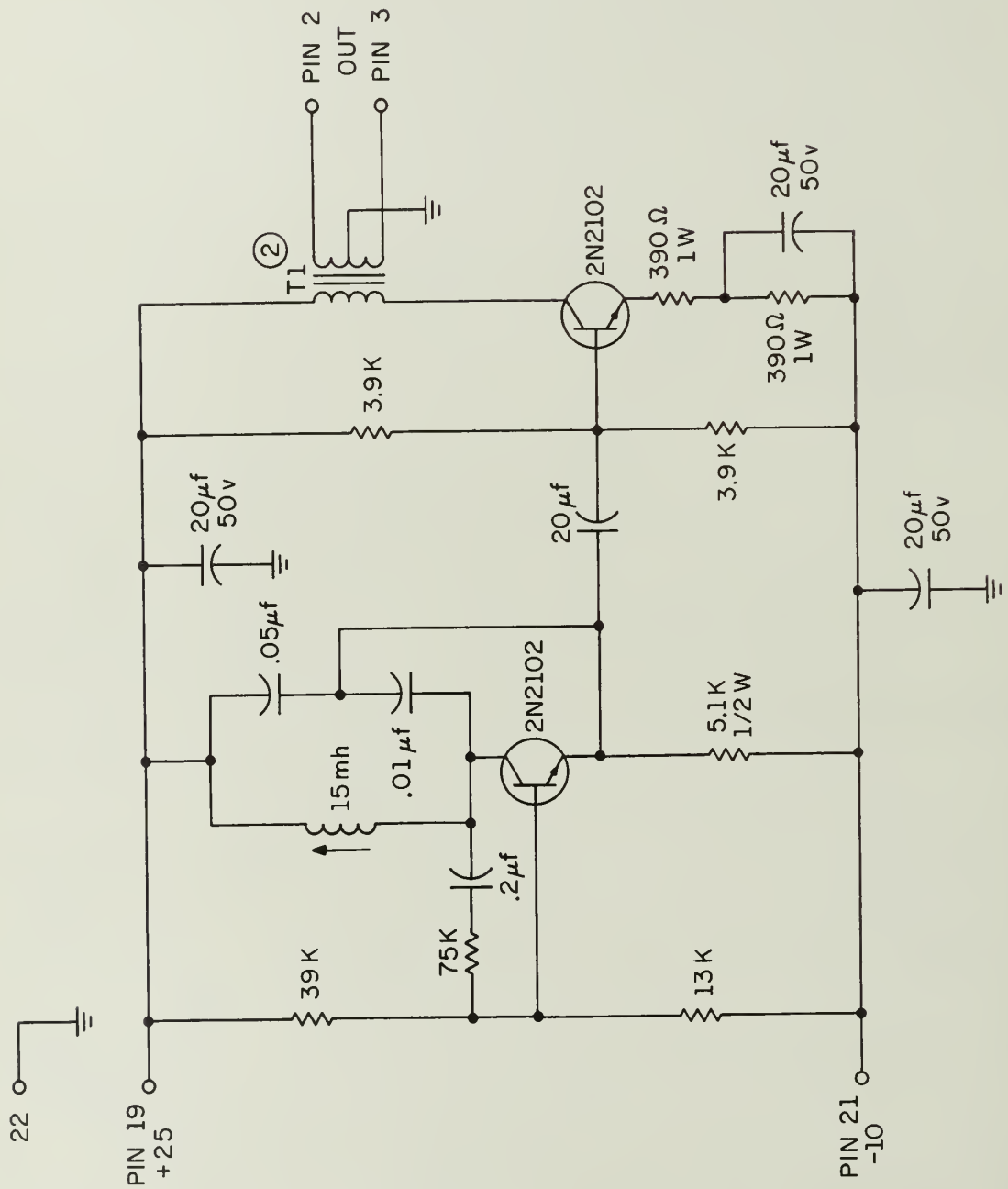
NOTES

1. ALL RESISTORS 1/4 W, 5%.

1469-152-07 DISPLAY GATE DRIVER

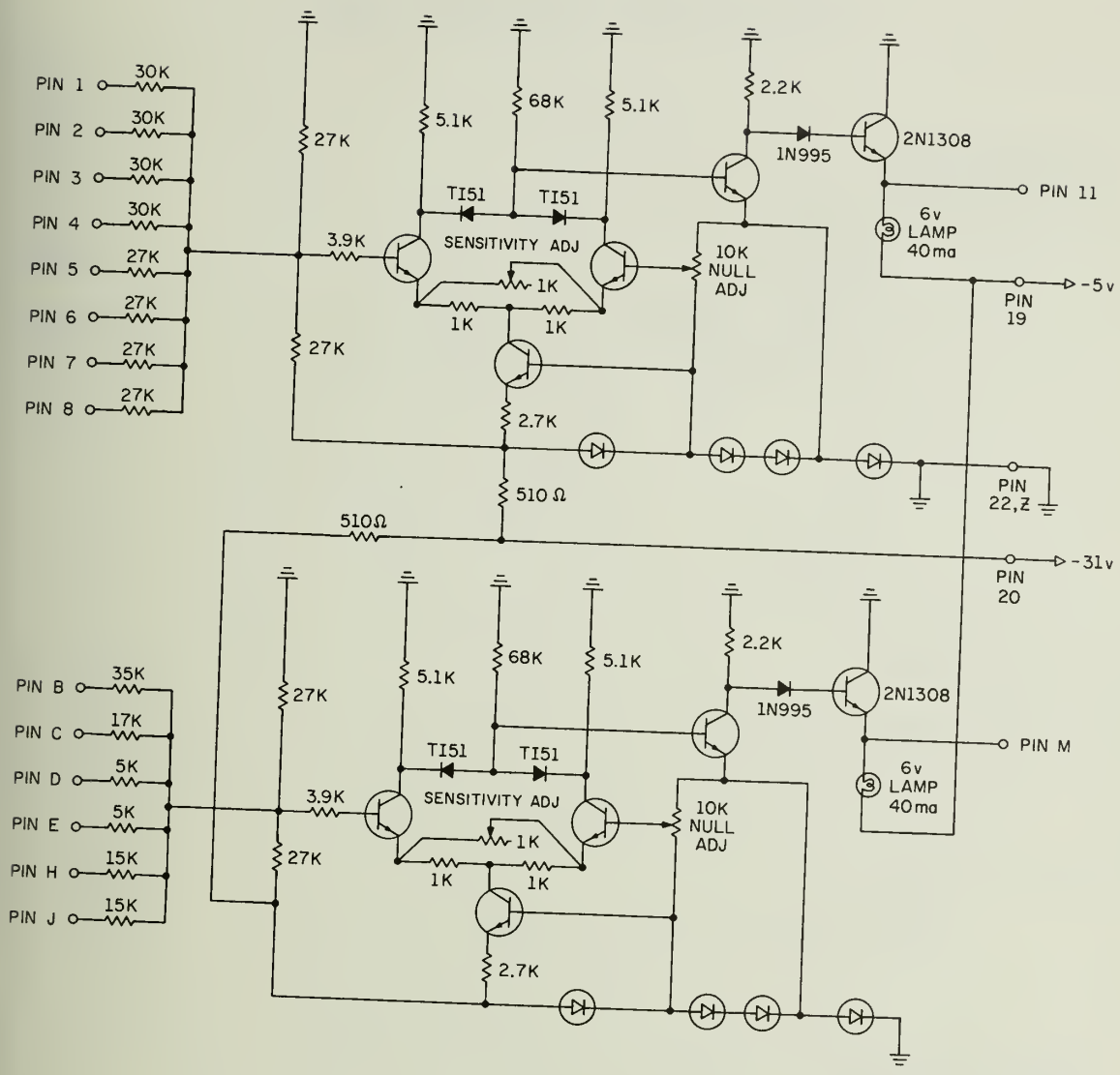


1469-153-00 10 Kc OSCILLATOR AND AMPLIFIER



NOTES

1. ALL RESISTORS 1/4 W, 5% UNLESS SPECIFIED.
2. T1: PRI → 100 Ω, SEC → 1000 Ω CT.

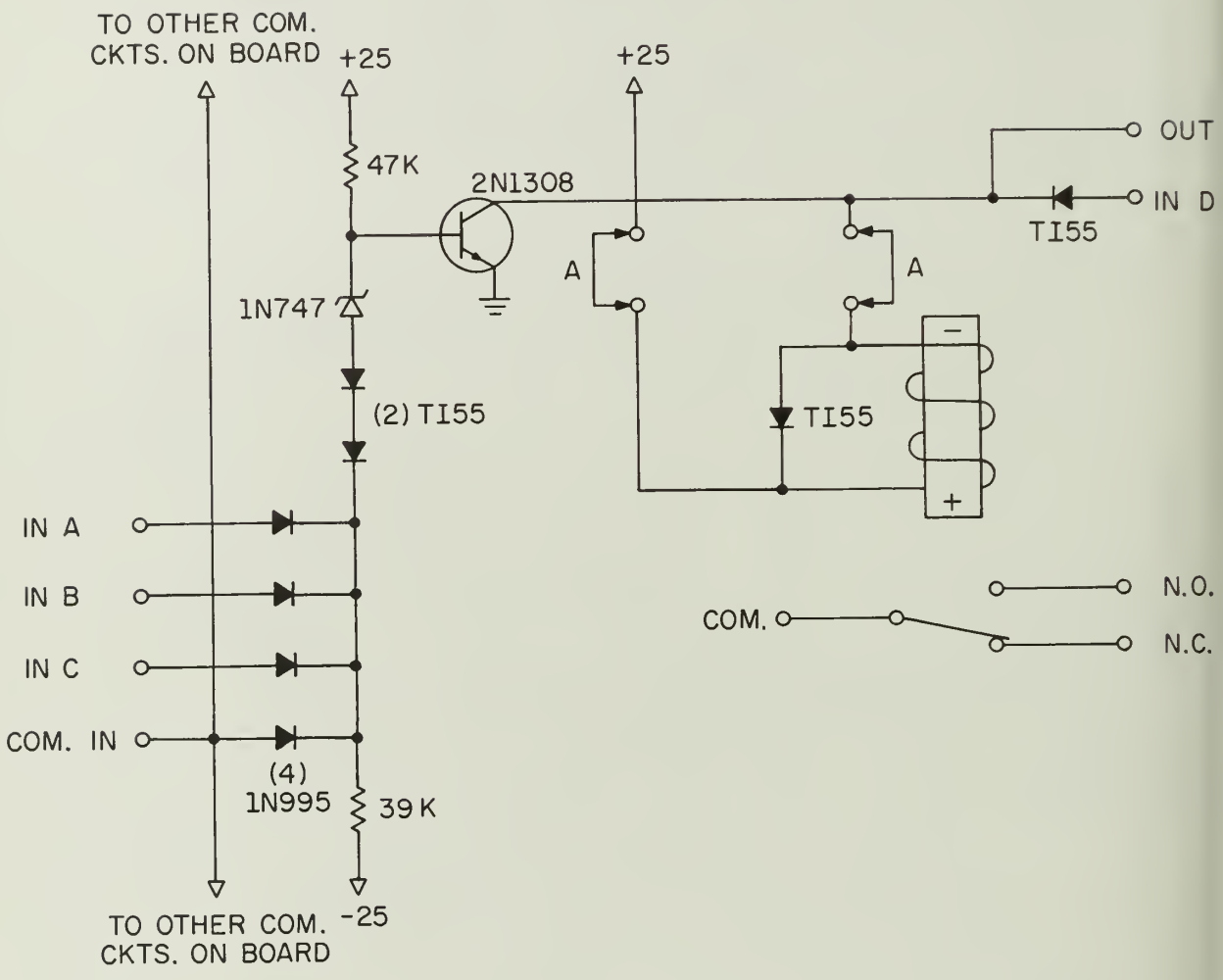


NOTES

1. ALL TRANSISTORS SM1530 UNLESS SPECIFIED.
2. ALL DIODES 1N751, 5v UNLESS SPECIFIED.

ARTRIX 1469-157 VOLTAGE MONITOR
HR-0010-0074

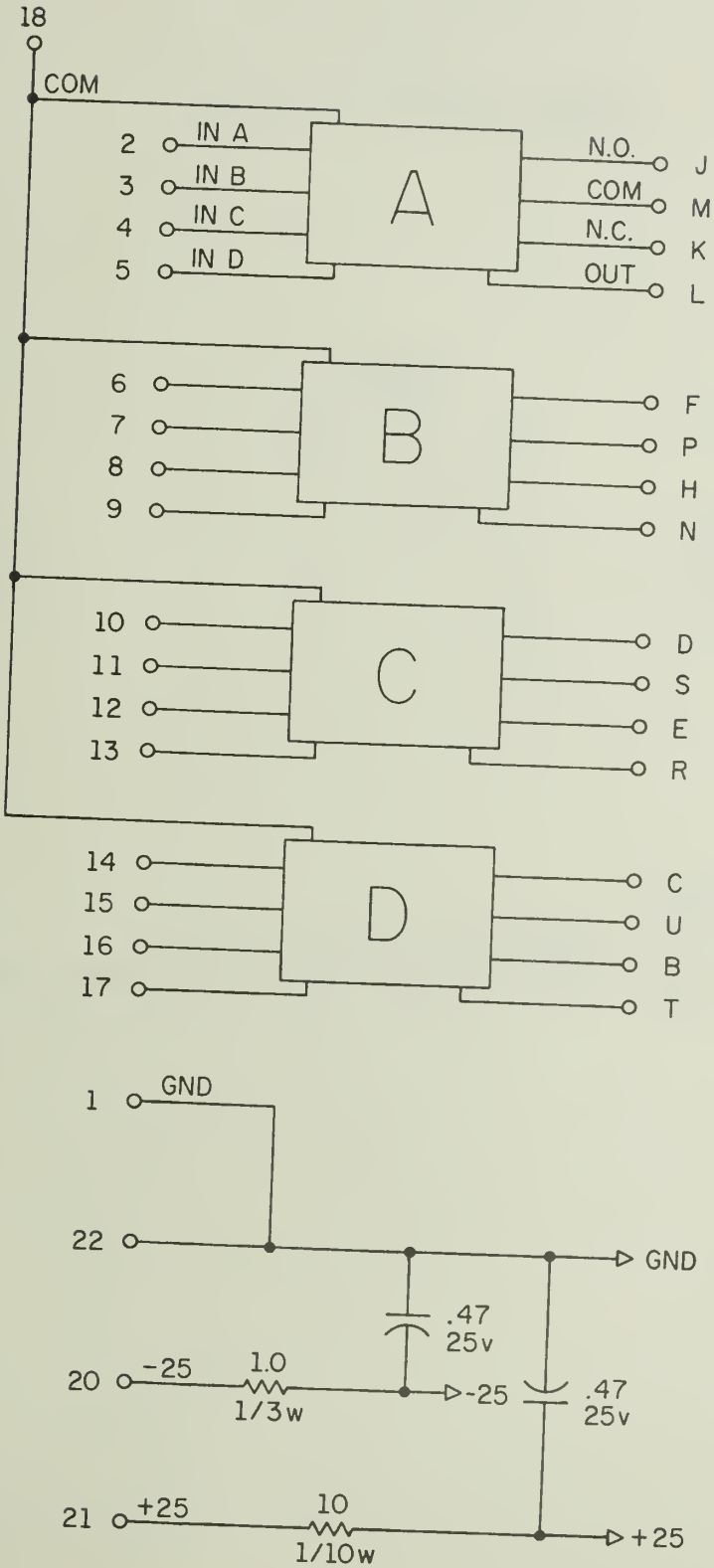
1469-164-00 Hg RELAY, SPDT



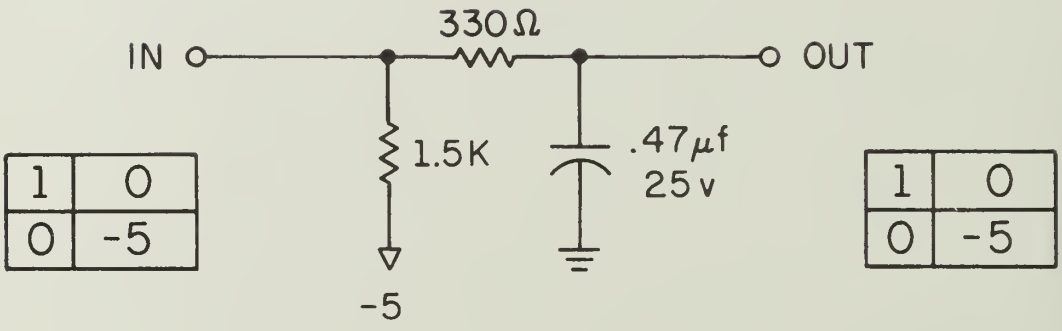
NOTES

1. ALL RESISTORS 1/4 W, 5%.
2. SEE NEXT PAGE FOR PIN CONNECTIONS.
3. RELAYS ARE MAGNECRAFT NO. W133MPCX-4 1000 Ω, 24 VOLT, Hg WETTED.

1469-164-00 Hg RELAY, SPDT



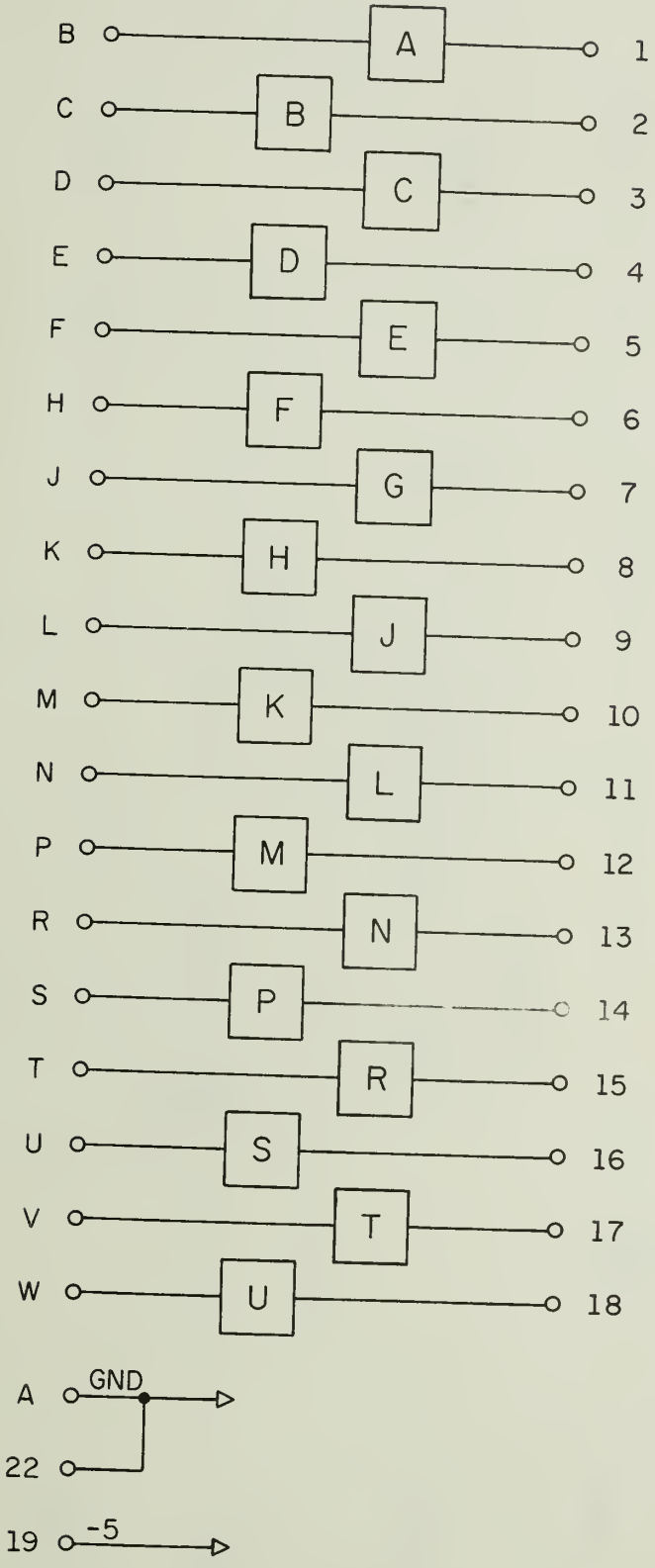
1469-173 FILTER



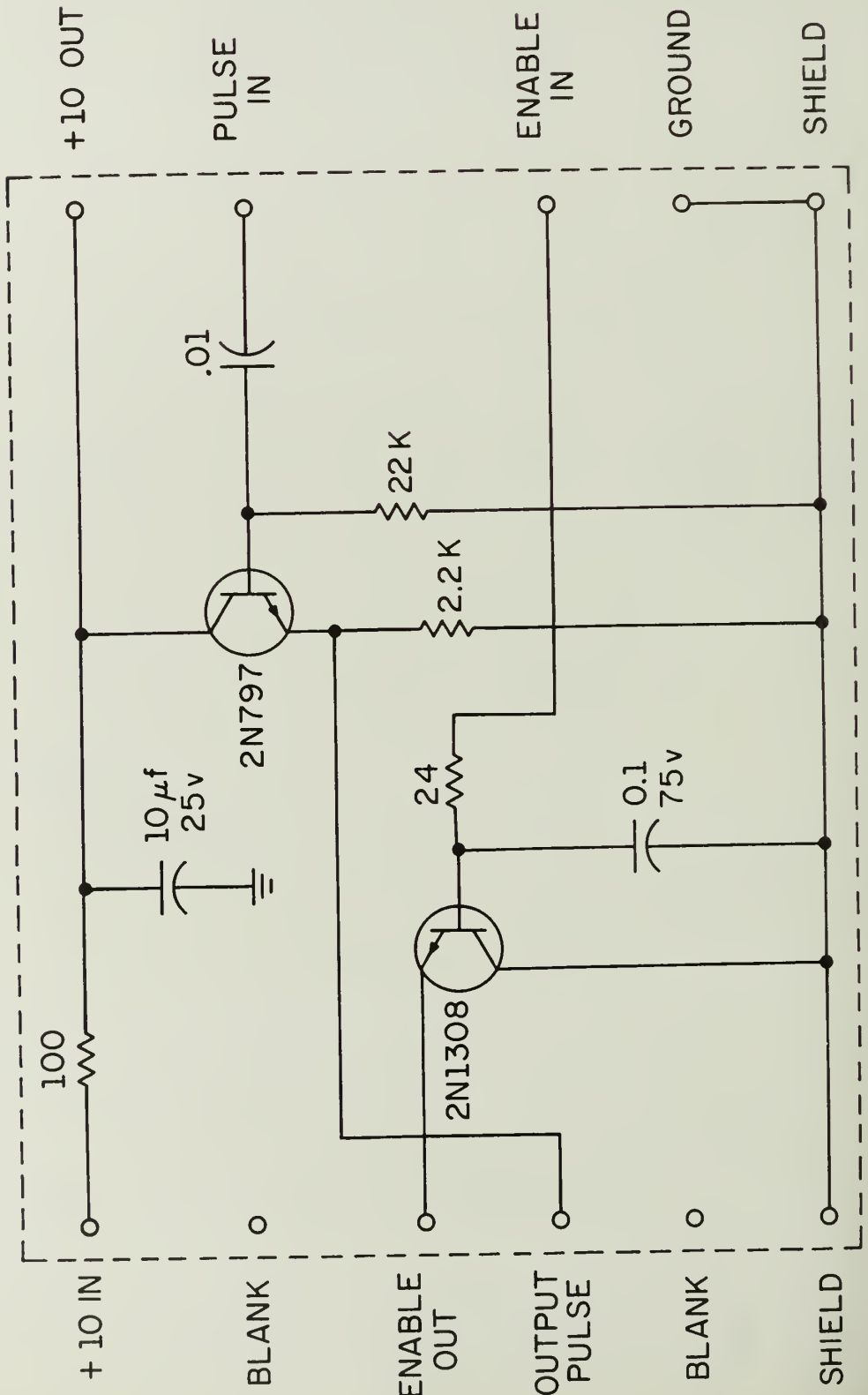
NOTES

1. ALL RESISTORS 1/4 W, 5%.
2. SEE NEXT PAGE FOR PIN CONNECTIONS.

1469-173 FILTER



LIGHT PEN CABLE DRIVER & ENABLE FILTER



A4.0 Physical Description

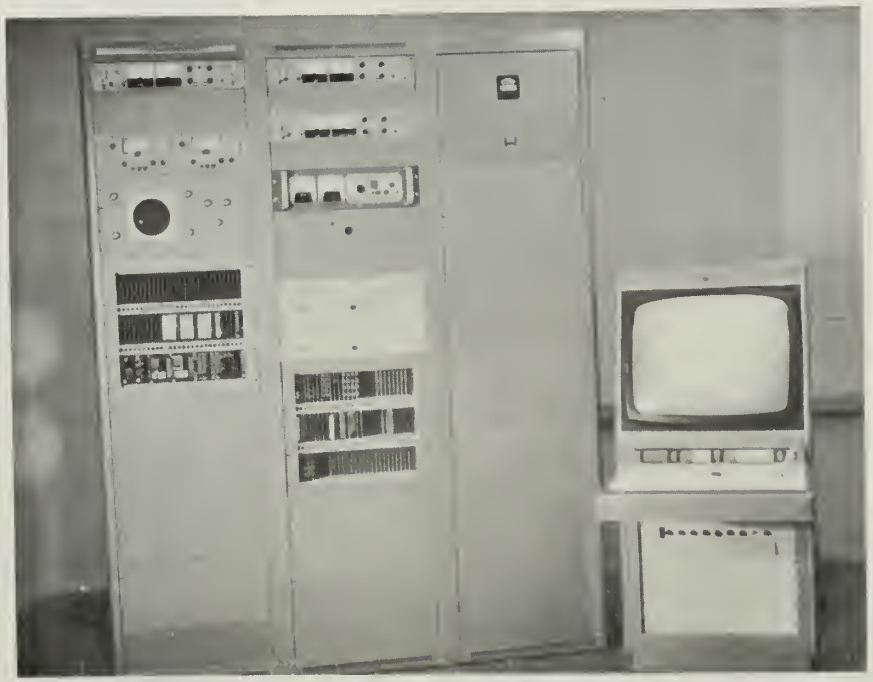


Figure A4.1 Complete ARTRIX System

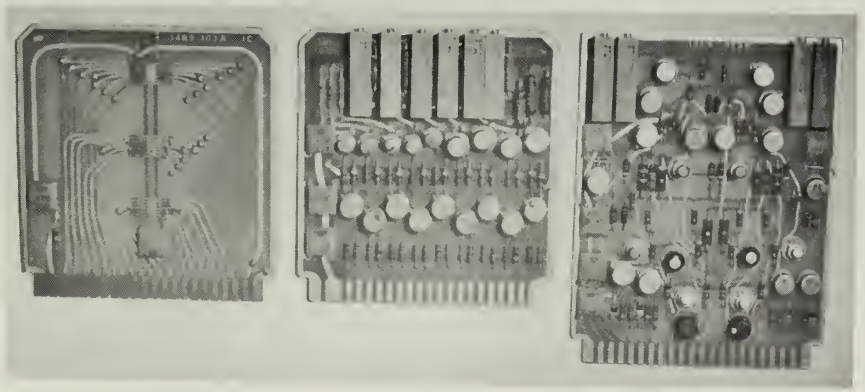


Figure A4.2 a Typical Circuit Boards, Front View

Figure A4.2 b Typical Circuit Boards, Rear View

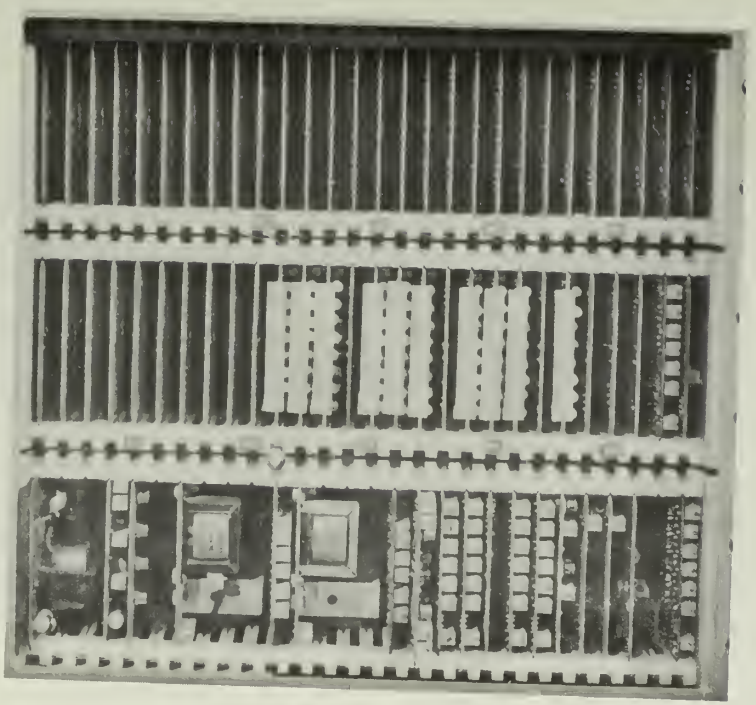


Figure A4.3 a Typical ARTRIX Printed Circuit Card Rack

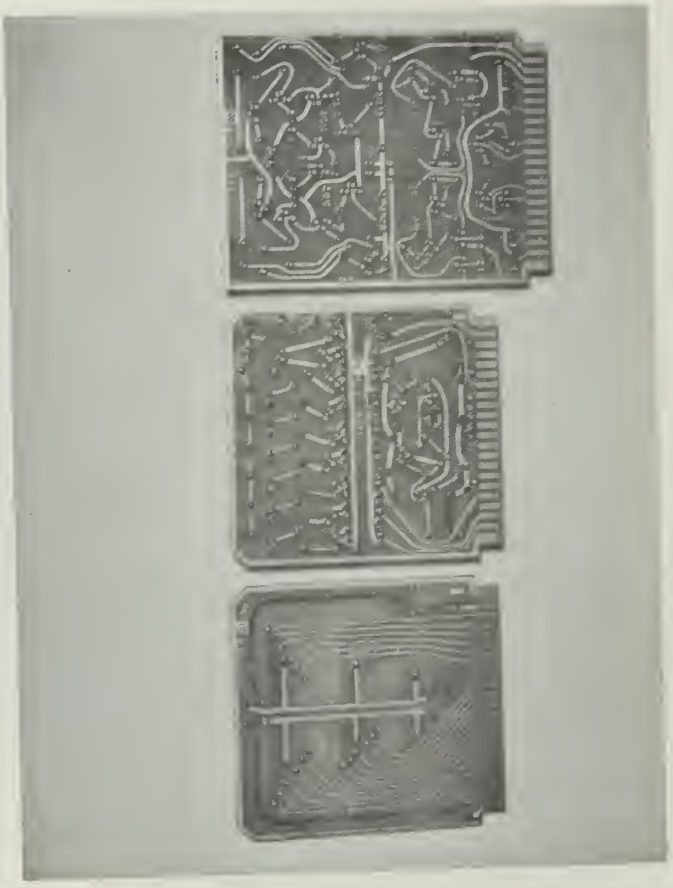


Figure A4.3 b Camera Control Rack

A5.0 Definition of PROCESSOR Logic Symbols

A_{i-j} Logical AND bits i through j.

$\overline{A}_{i-j}$ Logical AND NOT of the NOT side of bits i through j.

CH CH means complement Horizontal if a logical one.

$\underline{CH}$ Don't complement Horizontal if a logical one. $CH \cdot \underline{CH} = 0$.

CL_1 Because the gates have a limited fan out, the nine-bit

CL_2 counters need more than one signal to clear them. CL stands for Clear.

CR CR stands for Circle and is a logical one when the PROCESSOR is in the CIRCLE mode of operation.

CS CS stands for the Composite Synchronizing signal generated by the television CAMERA CONTROL UNIT.

CV CV means Complement Vertical if a logical one.

$\underline{CV}$ $\underline{CV}$ means don't complement Vertical if a logical one. $CV \cdot \underline{CV} = 0$.

E E stands for Equivalence and is a logical one when the two high order bits of the HORIZONTAL MASTER COUNTER are the same.

EF EF stands for Expanding Frequency and is the frequency which drives the EXPANDING RADIUS COUNTER.

ER ER stands for EXPANDING RADIUS COUNTER whose contents is the radius of circles drawn.

H_i H_i is the i^{th} bit of the digital signal which controls the Horizontal DCVGLA.

HM HM stands for Horizontal Master Counter whose contents correspond to the horizontal deflection in the television system.

HP_1 HP_1 stands for HORIZONTAL POINT 1 COUNTER and contains the horizontal coordinate of POINT 1.

HP_2 — HP_2 stands for HORIZONTAL POINT 2 COUNTER and contains the horizontal coordinate of POINT 2 for circles and the horizontal projection of the line for lines.

H_{coinc} — H_{coinc} stands for coicidence of the HORIZONTAL sweep with the horizontal coordinate for POINT 2.

LP — LP stands for LIGHT PEN pulse which occurs once each time the operator indicates a point on the DISPLAY in the POINT memory and pushes the ENABLE button.

OF — OF stands for Overflow and implies the condition that a Counter has gone from all ones to all zeros.

OP — OP stands for an operator-controlled signal.

PR — PR stands for PROCESSOR Reset and is a logical one when the PROCESSOR is reset.

PWG — PWG stands for PROCESSOR WRITE GATE and is a logical one when the PROCESSOR output is being written into the DISPLAY memory.

P_1 — P_1 stands for POINT 1 and is a logical one when POINT 1 has been indicated by the operator.

P_2 — P_2 stands for POINT 2 and is a logical one when POINT 2 has been indicated by the operator.

Q_i — Q_i is the i^{th} bit of a counter.

$\bar{Q}_i$ — $\bar{Q}_i$ is the NOT side of the i^{th} bit of a counter.

RP — RP stands for Reset PROCESSOR and is a logical zero when the PROCESSOR RESET button is pushed.

RR — RR stands for Reset Radius and is a logical zero when the RADIUS RESET Button is pushed.

RS — RS stands for Radius Stored and is a logical one when the proper radius for the circle has been found.

R_1 — R_1 stands for Reset POINT 1 and is a logical one when Horizontal and Vertical Point 1 Counters are being reset.

R_2 — R_2 stands for Reset POINT 2 and is a logical one when Horizontal and Vertical Point 2 Counters are being reset.

TH — TH stands for Trigger Horizontal and is the clocking signal for all Horizontal Counters.

TM — TM stands for Trigger Master and is the 8.064 MHz square wave.

TV — TV stands for Trigger Vertical and is the clocking signal for all Vertical Counters.

VB — VB stands for the Vertical Blanking signal generated by the television CAMERA CONTROL UNIT.

V_{coinc} — V_{coinc} stands for the coicidence of the Vertical Sweep with the Vertical Coordinate for Point 2.

V_i — V_i is the i^{th} bit of the digital signals which control the Vertical DCVGLA.

VM — VM stands for VERTICAL MASTER COUNTER whose contents correspond to the Vertical Deflection in the television system.

VP_1 — VP_1 stands for VERTICAL POINT 1 COUNTER and contains the Vertical Coordinate of Point 1.

VP_2 — VP_2 stands for VERTICAL POINT 2 COUNTER and contains the Vertical Coordinate of Point 2 for circles and the Vertical Projection of the line for lines.

XC — XC stands for Execute Construction and is a logical one when the Execute Construct Button is pushed.

XR — XR stands for Execute Ready and is a logical one when a construction is ready to be written into memory.

ηH — ηH is a logical one when the HORIZONTAL POINT 2 COUNTER is to count.

ηV — ηV is a logical one when the VERTICAL POINT 2 COUNTER is to count.

θ θ is a control signal for the VERTICAL POINT 2 COUNTER low order (least significant) bit. It is a logical one when that bit is to be triggered into the reset state.

ξH ξH is a logical one when the HORIZONTAL POINT 1 COUNTER is to count.

ξV ξV is a logical one when the VERTICAL POINT 1 COUNTER is to count.

Φ Φ is a Control Signal for the VERTICAL POINT 2 COUNTER low order (least significant) bit. It is a logical one when that stage is to be triggered into the set state.

A6.0 Alignment Procedure

Turn on ARTRIX and allow it to warm up for 1 hour.

A6.1 Memory Alignment

A6.1.1 Cameras

Adjust the four cameras per instruction found in Technical Manual, Code No. 6X-331(A), Operating and Maintenance Instructions for High-Resolution Closed Circuit Television Camera Controls, 3900 Series, Cohu Electronics, Incorporated, Box 623, San Diego, California 92112.

Make additional adjustments to insure that:

1) The face of the Memotron tube completely fills the monitor screen. This is accomplished by raising or lowering the camera and refocusing.

2) The camera is properly aligned rotationally such that vertical lines on the Memotron are vertical and horitzontal lines are horizontal on the monitor screen. This is accomplished by rotating the camera in its supporting frame.

3) The center of the Memotron screen is centered on the monitor screen. This is accomplished by centering the raster of the Vidicon in the camera.

Note that since only the POINT and DISPLAY video signals are normally displayed on the monitor it will be necessary to remove one of them and substitude TEMPORARY video in order to view the TEMPORARY memory. This is most easily accomplished at the camera outputs by interchanging cable 59 and 54 or 56. The ERASE memory can be viewed by switching to either erase mode.

Repeat any adjustment already made until the Vidicon-Memotron system is aligned, focussed, and gives proper output.

A6.1.2 Memo-Corders

The following adjustments must be made on the four Memo-Corders in ARTRIX. All adjustments are made while viewing

the video output of the respective memory displayed on the monitor. Again, cables must be substituted in the case of TEMPORARY.

1) Switch off the storage control in Memo-Corder being adjusted (for TEMPORARY, cables 31 and 34 are interchanged and an erase mode is used) and turn on the LIGHT PEN so that a spot is generated on the Memotron screen. Turn up intensity until pen spot is barely visible. Adjust focus and astigmatism for best spot size and shape.

2) Adjust threshold to the maximum setting which will still permit the storage surface to be erased.

A6.1.3 Horizontal and Vertical Gain and Position (Pen Alignment)

1) Before any alignment adjustments are made the vertical and horizontal sawtooth voltages generated by the vertical and horizontal sweep generator cards C2 and C3 must be adjusted. The adjustments are made by means of a potentiometer on the circuit boards. The horizontal peak to peak voltage output should be 20 volts. The vertical peak to peak voltage output should be 15 volts.

2) Draw horizontal lines at the top and bottom of the monitor and adjust the vertical gain and position controls of the Memo-Corder until the stored lines fall under the displayed pen spot vertically.

3) Draw vertical lines at the right and left of the monitor and adjust the horizontal position and gain controls of the Memo-Corder until the stored lines fall under the displayed pen spot horizontally.

4) Repeat 2 and 3 until the system tracks (i.e. when a point is written in any location of a memory it appears on the monitor under the displayed pen spot).

A6.2 PROCESSOR Alignment

A6.2.1 Tracking of POINT 1

Gain and position of DC levels of POINT 1.

1) Remove 10 KHz oscillator card and put the PROCESSOR in the CONSTRUCT LINE mode.

2) Put two points in the POINT memory, one 2 inches from the left edge of the screen and the other 2 inches from the right edge of the screen. Both should be placed about half way between top and bottom.

3) Reset the PROCESSOR and indicate the left hand point twice with the LIGHT PEN, storing it in the POINT 1 and POINT 2 registors. Push the XECUTE CONSTRUCT button and adjust the horizontal position of POINT 1 (potentiometer #3, card C17) until the line of zero length (a point) is aligned vertically with the left hand point in the POINT memory.

4) Reset the PROCESSOR and indicate the right hand point twice with the LIGHT PEN, storing it in the POINT 1 and POINT 2 registers. Push the XECUTE CONSTRUCT button and adjust the horizontal gain of POINT 1 (potentiometer #7, card C19) until the line of zero length (a point) is aligned vertically with the right hand point in the POINT MEMORY.

5) Repeat 3 and 4 of A6.2.1 until both points are aligned vertically with the points indicated in the POINT memory.

6) Put two points in the POINT memory, one two inches from the top of the screen, one two inches from the bottom of the screen. Both points should be placed about half way between the left and right hand edges of the screen. Repeat A6.2.1, 3, 4, and 5 for the vertical position of POINT 1 (potentiometer #2, card C17) and the vertical gain of POINT 1 (potentiometer #7, card C18). (Use the top point for the position adjustment and the bottom point for the gain adjustment).

A6.2.2 Length and Position Lines

1) Replace the 10 KHz oscillator card. Draw one pair of points, about one inch apart, one above the other, midway on the left hand edge of the screen. Similarly, draw a second set of points on the right hand edge of the screen. Construct one line connecting each of the top points,

indicating the right hand point first (POINT 1). Construct a second line connecting each of the bottom points indicating the left hand point first (POINT 1). Designate these lines RL and LR respectively.

2) Observe where RL falls in relation to LR. Repeat, indicating RL and LR while adjusting the $\Delta H/2$ gain control (potentiometer #7, Card C28) until the midpoints or RL and LR fall on a vertical axis. Observe also that LR will move faster than RL when the gain control is adjusted. Using RL as the reference line, align LR directly below RL.

3) Adjust the gain of RL and LR by changing the amplitude of the + sin(ωt) and - sin(ωt) sinusoids. (RL is - sin(ωt) potentiometer #3, Card C4, and LR is + sin(ωt), potentiometer #4, Card C4).

4) Draw one pair of points, about an inch apart, one beside the other, midway on the top edge of the screen. Similarly, draw a second set of points on the bottom edge of the screen. Construct a line connecting each of the left hand points, indicating the bottom point first (POINT 1). Construct a second line connecting each of the right hand points, indicating the top point first (POINT 1). Designate these lines BT and TB.

5) Repeat Parts 2 and 3 with BT and TB in place of RL and LR, until both BT and TB have their end points on horizontal lines. Use the $\Delta V/2$ gain control (potentiometer #7, B27). In this case, TB is the faster moving line.

6) Adjust the lengths of BT and TB with the aspect ratio control (potentiometer #1, Card C9). Both lengths are adjusted simultaneously with this control.

A6.2.3 Dummy Offset for Circles

1) Store a radius, then switch to the LINE mode and construct a line of zero length by indicating the same point twice (don't reset the radius when obtaining the line).

2) Pull the 10 KHz oscillator card.

3) One person must switch back and forth from the LINE to the CIRCLE mode, keeping the XECUTE CONSTRUCT button depressed.

A second person must adjust the horizontal dummy (potentiometer #4, Card C17) and the vertical dummy (potentiometer #1, Card C17) until the line of zero length and circle of zero radius coincide.

4) Replace the 10 KHz oscillator card.

A6.2.4 Shape and Size of Circles:

1) Construct a circle ten inches in diameter, and keep the XECUTE CONSTRUCT button depressed while the amplitude and phase of the COS(ω5) signal is adjusted to give a round circle (potentiometer #2, Card C4 and potentiometer #1, Card C4, respectively). Adjusting potentiometer #1, Card C4 may alter the lengths of the lines. Hence a readjustment of the lengths might be necessary.

2) Draw three points in a horizontal line, one in the center of the screen and the other four inches to the left and right of the first point. Indicate the center point as POINT 1 (in the CIRCLE mode) and the point on the left as POINT 2. Adjust potentiometer #2, Card C23 (position) until the circle passes through POINT 2. (Radius must be reset after each adjustment of the potentiometer, and circle must be rewritten). Now repeat the adjustment procedure with the right hand point and use potentiometer 7, Card C22 (gain) to make the circle pass through the right hand point. Repeat the entire procedure again to get even closer alignment. Similarly, draw three points in a vertical line. Using the center point as POINT 1, and using the top point as POINT 2, adjust potentiometer 1, Card C23 (position) until the circle passes through POINT 2. (Radius must be reset after each adjustment and a new circle must be rewritten). Similarly, using the lower point as POINT 2 adjust potentiometer 7, Card C21 (gain) until the circle passes through POINT 2. Repeat for greater accuracy.

A6.3 Memory Control Adjustment

Several adjustments are located on the Memory Control rack. These adjustments should be made when necessary.

A6.3.1 150 MILLISECOND MULTIVIBRATOR, Card B11

The potentiometers on this card should be adjusted such that the erase gate output is approximately 150 milliseconds.

A6.3.2 Pen Threshold Adjustment, card A1

The pen threshold potentiometer should be set for zero ohms unless a higher threshold level is desired for some reason.

A6.3.3 Video Adders, card A7 and A8

The video adder cards have four adjustments. These determine the relative amounts of the two inputs that are added together, the amplitude of the overall signal, and the synchronizing pulse amplitude.

At card A7 adjust for no synchronization output since no synchronization is added at this card. Adjust the relative amplitudes of the DISPLAY video input signal and the POINT video input signal such that the POINT video appears approximately twice as bright on the screen as the DISPLAY video. Adjust the overall gain to give a one volt video output level.

At card A8 adjust synchronization level to be 0.4 volts negative. Adjust the pen pulse and composite DISPLAY and POINT video signals such that the pen pulse amplitude is comparable to the POINT video level. Adjust the overall gain to give 1 volt of composite video (including synchronization).

A6.3.4 Discriminator Adjustment

Cards A12, A13, A14 and A15 are discriminators for the video outputs of the various memories. There are two discriminator circuits per card and two adjustments per circuit. These controls permit adjustments in the discrimination level and the output amplitude.

At card A12 the upper circuit controls the POINT video which reaches the TEMPORARY memory during the execute erase cycle. This circuit should be adjusted for the lowest possible discrimination level which will not allow background video to pass through the circuit. The output amplitude should be adjusted to the one volt level.

The lower circuit on card A12 should be set as above but for the DISPLAY memory.

Similarly, the upper and lower circuits on card A13 control the output video from the TEMPORARY memory which passes to the DISPLAY memory and the POINT memory, respectively. These circuits should be adjusted as above.

Similarly, the upper and lower circuits on A14 correspond to the video which passes from the ERASE memory to the DISPLAY memory and POINT memory, respectively. Adjust as above.

The lower circuit on card A15 is not used. The upper circuit controls the video level, above which, points in the POINT memory will be allowed to pass to the circuit which forms the logical AND of the pen pulse and the points in the POINT memory. The discrimination level should be set as low as possible without allowing indiscrimate pulses to pass through this circuit to the logic. The output level should be set to the one volt level.

A6.3.5 Erase Level Adjustment

When in the ERASE DISPLAY mode, adjust the synchronization level on the DISPLAY video circuit board of the DISPLAY CAMERA CONTROL UNIT such that an erase point in the ERASE memory causes the video to be lowered just to the black level.

Similarly, in the ERASE POINT mode adjust the synchronization level of the POINT video circuit board in the POINT CAMERA CONTROL SITE.